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IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

SEMICONDUCTOR ENERGY LABORATORY COMPANY, LTD.,

Plaintiff,

v.

ACER INCORPORATED, ACER AMERICA CORPORATION, and AU OPTRONICS CORPORATION,

Defendants.

CASE NO. C 02-02800 WHA

JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT

Pursuant to Patent L.R. 4-3, Plaintiff Semiconductor Energy Laboratory Company, Ltd. ("SEL") and Defendants Acer Incorporated, Acer America Corporation

(collectively "Acer") and AU Optronics Corporation ("AU"), through their respective counsel, hereby jointly submit the following "Joint Claim Construction and Prehearing Statement."

1. Agreed Claim Constructions (L.R. 4-3(a))

The parties' counsel have met and conferred but the parties do not agree on the construction of any disputed claim terms, phrases or clauses. The parties also do not agree on which terms should be construed for the Claim Construction Hearing set for April 9, 2003.

2. Anticipated Length of Claim Construction Hearing (L.R. 4-3(c))

The parties agree that the anticipated time necessary for the Claim Construction Hearing is one day.

3. Proposed Constructions and Identification of Evidence, Witnesses and Other Issues (L.R. 4-3(b),(d) and (e))

A. SEL's Proposed Constructions and Identification of Evidence, Witnesses and Other Issues (L.R. 4-3(b),(d) and (e))

SEL proposed that the claim phrase "wherein said conductive adhesive extends lengthwise beyond each end of the first and second electrodes" and the claim phrase "each end of said first electrode and said second electrode is completely covered by said resin in a lengthwise direction" from U.S. Patent No. 6,404,476 be construed. The Defendants proposed that five additional claim terms or phrases from the patents in suit be construed. Pursuant to Patent Local Rule 4-3(b), SEL's proposed claim constructions for the terms and phrases proposed by all parties are given below for each patent. Following each construction, the intrinsic evidence and extrinsic evidence in support of SEL's construction or in opposition to Defendants' constructions is identified per Patent Local Rule 4-3(d). Finally, other issues relevant to the Claim Construction Hearing are raised pursuant to Patent Local Rule 4-3(e).

U.S. Patent No. 6,404,476 (the "'476 patent")

(1) The phrase **"wherein said conductive adhesive extends lengthwise beyond each end of the first and second electrodes"** should be construed to mean: wherein said conductive adhesive extends lengthwise beyond an end of the first electrode and an end of the second electrode.

In addition to intrinsic evidence, including the intrinsic evidence listed in attached Exhibit A, SEL may rely on the testimony of Paul Kohl, Ph.D., who will testify that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the specification and prosecution history of the '476 patent and any related applications, and any references cited therein. Dr. Kohl will also testify that Defendants' proposed claim constructions, as viewed by one of ordinary skill in the art, are not in accordance with the intrinsic evidence. Dr. Kohl's curriculum vitae is attached in Exhibit B.

(2) The phrase **"each end of said first electrode and said second electrode is completely covered by said resin in a lengthwise direction"** should be construed to mean: an end of said first electrode and an end of said second electrode is completely covered by said resin in a lengthwise direction.

In addition to intrinsic evidence, including the intrinsic evidence listed in attached Exhibit A, SEL may rely on the testimony of Paul Kohl, Ph.D., who will testify that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the specification and prosecution history of the '476 patent and any related applications, and any references cited therein. Dr. Kohl will also testify that Defendants' proposed claim constructions, as viewed by one of ordinary skill in the art, are not in accordance with the intrinsic evidence.

U.S. Patent No. 6,355,941 (the "'941 patent")

(1) The phrase **"non-single crystal semiconductor"** should be construed to mean: a semi-amorphous semiconductor, an amorphous semiconductor or a mixture thereof.

In addition to intrinsic evidence, including the intrinsic evidence listed in Exhibit A, SEL may rely on testimony of Rafael Reif, Ph.D., who will testify that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the specification and prosecution history of the '941 patent and any related applications, and any references cited therein. Dr. Reif will also testify that the Defendants' proposed claim constructions, as viewed by one of ordinary skill in the art, are not in accordance with the intrinsic evidence. Dr. Reif's curriculum vitae is attached in Exhibit B.

(2) The term **"intrinsic"** should be construed to mean: not intentionally doped with an efficient dopant.

In addition to intrinsic evidence, including the intrinsic evidence listed in Exhibit A, SEL may rely on testimony of Rafael Reif, Ph.D., who will testify that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the specification and prosecution history of the '941 patent and any related applications, and any references cited therein, and that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is supported by the extrinsic evidence, including the extrinsic evidence cited in Exhibit A. Dr. Reif will also testify that the Defendants' proposed claim constructions, as viewed by one of ordinary skill in the art, are not in accordance with the intrinsic and extrinsic evidence.

(3) The phrase **"channel region (or channel forming region)"** should be construed to mean: an area extending from the source to drain, including but not limited to, the channel.

In addition to intrinsic evidence, including the intrinsic evidence cited in Exhibit A, SEL may rely on testimony of Rafael Reif, Ph.D., who will testify that SEL's proposed claim

construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the specification and prosecution history of the '941 patent and any related applications, and any references cited therein. Dr. Reif will also testify that the Defendants' proposed claim constructions, as viewed by one of ordinary skill in the art, are not in accordance with the intrinsic evidence.

U.S. Patent No. 6,404,480 (the "'480 patent")

(1) The phrase **"second interlayer insulating film having at least two openings"** should be construed to mean: the second interlayer insulating film has at least two openings, as shown, for example in Figs. 1, 2A, 5F, 5G and 6-11 of the '480 patent.

In addition to intrinsic evidence, SEL may rely on the testimony of Paul Kohl, Ph.D., who will testify that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the specification and prosecution history of the '480 patent and any related applications, and any references cited therein. Dr. Kohl will also testify that Defendants' proposed claim constructions, as viewed by one of ordinary skill in the art, are not in accordance with the intrinsic evidence.

U.S. Patent No. 5,929,527 (the "'527 patent")

(1) The phrase "the film made of aluminum or a material containing aluminum as a principal component contains oxygen atoms at a concentration of $8x10^{18}$ atoms•cm^{-3} or less, carbon atoms at a concentration of $5x10^{18}$ atoms•cm^{-3} or less, and nitrogen atoms at a concentration of $7x10^{17}$ atoms•cm^{-3} or less" is readily understood and the terms therein should be accorded their plain meaning.

The Defendants proposed claim constructions are not in accordance with the plain meaning of the claim terms, as viewed by one of ordinary skill in the art. The intrinsic evidence, including the intrinsic evidence cited in Exhibit A, the specification and prosecution

history of the '527 patent and any related applications, and any references cited therein supports SEL's proposed construction. The Defendants have not identified any extrinsic evidence in support of their proposed claim constructions and SEL reserves the right to rebut any extrinsic evidence identified by Defendants with extrinsic evidence, including expert testimony.

Other Claim Construction Issues

The parties have a dispute as to what should be disclosed in this Joint Claim Construction Statement. Consistent with Patent L.R. 4-3, in this Joint Statement, SEL has attempted to identify all intrinsic and extrinsic evidence it may rely upon in support of its proposed claim constructions. Defendant AU Optronics has advised SEL that it is reserving its rights to offer extrinsic evidence that it has not yet identified until such time as the Court has ruled on the admissibility of extrinsic evidence. SEL has objected to this approach, and instead interprets Patent L.R. 4-3 to require the parties to disclose any evidence that they may use as part of the claim construction process. Defendants Acer have advised SEL that they are reserving their rights to offer extrinsic evidence only in rebuttal. Although AU Optronics asserts that the Court should review only intrinsic evidence, if the Court decides to review extrinsic evidence for any purpose, including any expert testimony, that extrinsic evidence should be identified now, not at the claim construction hearing. Otherwise, SEL's ability to complete claim construction discovery prior to the claim construction hearing would be frustrated.

B. Acer's Proposed Constructions and Identification of Evidence, Witnesses and Other Issues (L.R. 4-3(b),(d) and (e))

Acer reserves the right, pursuant to Patent L.R. 4-3(b), to rely upon additional intrinsic evidence, including but not limited to portions of the prosecution history of the Patents-in-Suit and related patents, to oppose SEL's proposed constructions of disputed claim terms.

U.S. PATENT NO. 6,355,941

Claim Term	Proposed Construction	Support
Non-single crystal semicondutor	The term "non-single crystal semiconductor" means "semiconductor material having lattice strain."	Col. 1, lines 23-29; Col. 7, lines 25-28; Col. 8, lines 25-30; May 3, 1991 Third Preliminary Amendment, pp. 4-6; December 12, 1991 Amendment, pp. 8-11 and Appx. I-II; March 5, 1992 Office Action, p. 3; January 8, 1993 Preliminary Amendment, pp. 4-6; January 26, 1993 Declaration, pp. 1-9; August 13, 1993 Supplemental Preliminary Response, pp. 2-4; July 14, 1994 Office Action, p. 2
Intrinsic	The term "intrinsic" means that the non-single crystal semiconductor material has the charge-carrier concentration of a pure, ideal crystal of that material.	"A semiconductor whose charge-carrier concentration is substantially the same as that of the ideal crystal." *IEEE Standard Dictionary of Electrical and Electronics Terms*, Sixth Edition. Col. 8, lines 3-8; May 3, 1991 Third Preliminary Amendment, p. 8; December 2, 1994 Amendment, pp. 8-9

Channel region	The term "channel region" means "a semiconductor layer connecting and conducting current between the drain region and the source region."	"A surface layer of carriers connecting source and drain in an insulated-gate field-effect transistor." *IEEE Standard Dictionary of Electrical and Electronics Terms*, Sixth Edition. Col. 11, lines 39-45; Fig. 6H

U.S. PATENT NO. 6,404,480

Claim Term	Proposed Construction	Support
Second interlayer insulating film having at least two openings	The term "at least two openings" means "two holes in the contact structure located in the common contact portion."	Abstract; Field of Invention; Summary of Invention; Fig. 1, & 5-8; col. 5, line 46 to col. 6, 42; Fig. 1; col. 9, line 60-67; col. 10, lines 24-49.

U.S. PATENT NO. 5,929,527

Claim Term	Proposed Construction	Support
The film made of aluminum or a material containing aluminum as a principal component contains oxygen atoms at a concentration of $8x10^{18}$ atoms▲cm^{-3} or less, carbon atoms at a concentration of $5x10^{18}$ atoms·cm^{-3} or less, and nitrogen atoms at a concentration of $7x10^{17}$ atoms·cm^{-3} or less	This phrase means "the maximum concentration of oxygen cannot exceed $8x10^{18}$ atoms·cm^{-3} at any point in the thin film containing aluminum as a principal component, the maximum concentration of carbon cannot exceed $5x10^{18}$ atoms·cm^{-3} at any point in the thin film containing aluminum as a principal component, and the maximum concentration of nitrogen cannot exceed $7x10^{17}$ atoms·cm^{-3} at any point in the thin film containing aluminum as a principal component."	Col. 7, line 30 to col. 8, line 11.

U.S. PATENT NO. 6,404,476

Claim Term	Proposed Construction	Support
Wherein said conductive adhesive extends lengthwise beyond each end of the first and second electrodes	The term "first electrode" means "an electrode strip formed on the first substrate for conducting electrical current" and the term "second electrode" means "an electrode strip contained in the circuit for supplying driving signals."	Fig. 1, 2, & 3. Col. 2, line 57 to col. 4, line 43.
Each end of said first electrode and said second electrode is completely covered by said resin in a lengthwise direction	The term "first electrode" means "an electrode strip formed on the first substrate for conducting electrical current" and the term "second electrode" means "an electrode strip contained in the circuit for supplying driving signals."	Fig. 1, 2, & 3. Col. 2, line 57 to col. 4, line 43.

C. AU's Proposed Constructions and Identification of Evidence, Witnesses and Other Issues (L.R. 4-3(b),(d) and (e))

AU Optronics presents the following Proposed Construction and Identification of Evidence pursuant to the requirements of the Court's September 11, 2002 Case Management Order limiting the number of terms to be construed at the claim-construction hearing. AU Optronics reserves the right to seek, and will seek, construction of additional claim terms and phrases at trial, or at another time, as directed by the Court. AU Optronics' submission is based upon information currently available to AU Optronics. As additional information becomes available through discovery, AU Optronics reserves the right to amend and/or supplement its Proposed Constructions and Identification of Evidence, Witnesses and Other Issues. AU Optronics further reserves the right to amend and/or supplement its position on claim construction once AU Optronics has had the opportunity to review any future finding or order from the Court related to construction of claim-terms.

I. U.S. PATENT NO. 6,355,941

AU Optronics identifies the following phrase in asserted independent claims 3, 6, 10, 11, 12, 13, 14, 15, 16, 20 and 21 of U.S. Patent No. 6,355,941 ("the '941 patent") for which it contends that construction by the Court is necessary:

"*. . . non-single crystal semiconductor . . .*"

AU Optronics contends that the phrase "*non-single crystal semiconductor*" was defined by the inventor during prosecution to mean that a "*non-single crystal semiconductor*" is a semi-amorphous material that includes microcrystalline structures that have lattice strain and which

are dispersed within an amorphous semiconductor material such that the "*non-single crystal semiconductor*" is different from both amorphous or polycrystalline semiconductor materials.

As examples of intrinsic evidence upon which AU Optronics may rely, AU Optronics cites the following from the prosecution history of the '941 patent: U.S. Patent Appl. Ser. No. 06/237,609, Application filed February 24, 1981, p. 9, l. 20 – p. 10, l. 3; *id.*, p. 11, ll. 1-12; *id.*, p. 12, ll. 14-18; *id.*, p. 36; *id.*, Fig. 2; U.S. Patent Appl. Ser. No. 06/237,609, Amendment filed December 13, 1982, p. 4; U.S. Patent Appl. Ser. No. 06/278,418, Application filed June 29, 1981, p. 8, ll. 2-6; *id.*, p. 15, ll. 7-15; *id.*, p. 17, l. 22 – p. 18, l. 6; p. 19, l. 12 – p. 20, l. 23; *id.*, p. 24, l. 12 – p. 25, l. 7; *id.*, p. 28, l. 24 – p. 29, l. 4; *id.*, p. 32, ll. 21-24; *id.*, p. 33, ll. 2-6; *id.*, Fig. 5; *id.*, Figs. 6D-6H (as found in PTO file); Translation of Japanese Patent Application No. 55-088974, pp. 2, 6, 7-8, 10, 11, 12, 14, 15, 16, 17, 18, 19; U.S. Patent Appl. Ser. No. 06/278,418, Amendment filed August 28, 1985, pp. 2-3, 5, 6; U.S. Patent Appl. Ser. No. 06/278,418, Amendment filed September 12, 1985, pp. 3, 4, 5; U.S. Patent Appl. Ser. No. 06/775,767, Amendment filed September 13, 1985, p. 5; Office Action mailed July 22, 1986, p. 3; U.S. Patent Appl. Ser. No. 07/488,102, Amendment filed March 28, 1991, pp. 1-5; U.S. Patent Appl. Ser. No. 07/488,102, Amendment filed May 2, 1991, pp. 2-11; U.S. Patent Appl. Ser. No. 07/602,167, Amendment filed October 23, 1990, pp. 1-2; U.S. Patent Appl. Ser. No. 07/602,167, Amendment filed May 2, 1991, pp. 4-9; U.S. Patent Appl. Ser. No. 07/602,167, Office Action mailed June 13, 1991, p. 2; U.S. Patent Appl. Ser. No. 07/602,167, Amendment filed December 12, 1991, pp. 7-11 and Appendices I & II; U.S. Patent Appl. Ser. No. 08/098,548, Amendment filed January 8, 1993, pp. 3-8; U.S. Patent Appl. Ser. No. 08/098,548, Declaration of Shunpei Yamazaki, dated January 21, 1993; U.S. Patent Appl. Ser. No. 08/098,548, Supplemental Response filed August 13, 1993, pp. 1-4; U.S. Patent Appl. Ser. No. 08/098,548, Amendment filed April 22, 1994, pp. 1-9; U.S. Patent Appl. Ser. No. 08/098,548, Office Action mailed July 14, 1994, pp. 2-5; U.S. Patent Appl. Ser. No. 08/098,548, paper no.

24, Interview Summary; U.S. Patent Appl. Ser. No. 08/098,548, Amendment filed December 2, 1994, pp. 2-13; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed January 11, 1995, pp. 2-13; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed June 21, 1995, pp. 1-16; U.S. Patent Appl. Serial No. 08/371,486, Supplemental Information Disclosure Statement and Response, filed October 17, 1995, pp. 1-4; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed May 29, 1996, pp. 8-14 and Appendix I; U.S. Patent Appl. Serial No. 08/371,486, paper no. 46, Interview Summary, Proposed Claims, pp. 9-11; U.S. Patent Appl. Serial No. 08/371,486, Declaration of Shunpei Yamazaki, dated April 10, 1997; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed April 27, 1997, pp. 10-12, 18-21; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed January 22, 1998, pp. 1-3; U.S. Patent Appl. Serial No. 08/371,486, Appeal Brief filed April 16, 1998, pp. 4-5, 7, 8, 10-13, 15-17; and U.S. Patent No. 6,355,941, col. 3, ll. 40-44; *id.*, col. 6, ll. 21-29; *id.*, col. 7, ll. 19-28; *id.*, col. 7, l. 60 – col. 8, l. 30; *id.*, col. 9, l. 54 – col. 10, l. 8; *id.*, col. 11, ll. 34-38; *id.*, col. 12, ll. 62-65; *id.*, col. 13, ll. 1-5; *id.*, Fig. 5; Figs. 6D-6H.

As additional intrinsic evidence upon which AU Optronics may rely, AU Optronics cites the following references from the prosecution history files of the '941 patent: U.S. Patent No. 3,191,061; U.S. Patent No. 3,265,981; U.S. Patent No. 3,271,632; U.S. Patent No. 3,339,128; U.S. Patent No. 3,585,088; U.S. Patent No. 3,644,741; U.S. Patent No. 3,716,844; U.S. Patent No. 3,771,026; U.S. Patent No. 3,988,720; U.S. Patent No. 3,999,212; U.S. Patent No. 4,062,034; U.S. Patent No. 4,117,506; U.S. Patent No. 4,217,374; U.S. Patent No. 4,224,084; U.S. Patent No. 4,225,222; U.S. Patent No. 4,226,898; U.S. Patent No. 4,236,167; U.S. Patent No. 4,239,554; U.S. Patent No. 4,240,843; U.S. Patent No. 4,254,429; U.S. Patent No. 4,270,018; U.S. Patent No. 4,272,880; U.S. Patent No. 4,317,844; U.S. Patent No. 4,339,285; U.S. Patent No. 4,398,343; U.S. Patent No. 4,485,389; U.S. Patent No. 4,605,941; Translation of Published Japanese Patent Application No. 55-11329; Translation of Published Japanese

Patent Application No. 55-11330; Translation of Published Japanese Patent Application No. 55-11330; Translation of Published Japanese Patent Application No. 55-11329; Translation of Published Japanese Patent Application No. 55-13938; Translation of Published Japanese Patent Application No. 55-13939; Japanese Published Patent Application No. 54-152894; Japanese Published Patent Application 55-050663; Japanese Published Patent Application 55-050664; W.E. Spear and P. G. Le Comber, "Electronic Properties of Substitutionally Doped Amorphous Si and Ge", Philosophical Magazine, 1976, vol. 33. N. 6, 935-949; S.M. Sze, Physics of Semiconductor Devices, pp. 568-621 (1969); M. Hirose, T. Suzuki, and G. H. Döhler, "Electronic Density of States in Discharge-Produced Amorphous Silicon," Applied Physics Letters, Vol. 34, No. 3, pp. 234-236 (Feb. 1, 1979); Nakamura et al., "Characteristics of Amorphous silicon TFTs," Extended Abstracts (The 40th Autumn Meeting), The Japan Society of Applied Physics, p. 325, 30P-S-17 (Sep. 1979); M. Hirose, T. Suzuki, and G. H. Doehler, "Determination of Localized State Density Distribution in Glow Discharge Amorphous Silicon," Proceedings of the 10th Conference on Solid State Devices, JAP, vol. 18, pp. 109-113 (1979); Matsumura et al., "a-Si Thin Film MOS Transistor," Extended Abstracts (The 40th Autumn [sic?] Meeting), The Japan Society of Applied Physics, p. 326, 30P-S-18 (1979); Hiroshi Hayama and Masakiyo Matsumura, "Amorphous-Silicon Thin-Film Metal Oxide-Semiconductor Transistors," Applied Physics Letter, pp 754-755 (May 1980); M. Matsumura, "Amorphous Silicon Thin-Film Electro Devices," The Japan Society of Applied Physics, vol. 49, No. 7, pp 729(81)-732(84) (July 10, 1980); A. F. Tasch, Jr., T. C. Holloway, K. F. Lee, J. F. Gibbons, "Silicon-on-Insulator M.O.S.F.E.T.S. Fabricated on Laser-Annealed Polysilicon on SiO_2," Electronics Letters, Vol. 15, No. 14, pp. 435-437 (Jul. 1979); A. Matsuda et al., "Electrical and Structural Properties of Phosphorus-Doped Glow-discharge Si:F:H and Si:H Films" Japanese Journal of Applied Physics, vol. 19, No. 6, Jun., 1980, pp. L305-L308; A. Madan, P. G. Le Comber and W.E. Spear, "Investigation of the Density of Localized States in a-

Si Using the Field Effect Technique," J. of Non-Crystalline Solids 20, pp. 239-257 (1976); Hiroshi Hayama and Masakiyo Matsumura, "a-Si FET IC Integrated on a Glass Substrate," National Convention Record, The Institute of Electronics and Communication Engineers of Japan, S3-13, pp. 2-287 to 2-288 (Mar. 1980); T. I. Kamins, "Field-Effects in Polycrystalline-Silicon Films," Solid-State Electronics, Vol. 15, pp 789-799 (Jul. 1972); Masakiyo Matsumura and Yasuo Nara, "a-Si P Channel FET," National Convention Record, The Institute of Electronics and Communication Engineers of Japan, pp. 2-281-282, S3-10 (Mar. 1980); W. E. Spear and P. G. Le Comber, "Substitutional Doping of Amorphous Silicon," Solid State Communications, vol. 17, No. 9, pp. 1193-1196 (Nov. 1975); Hiroshi Hayama and Masakiyo Matsumura, "Amorphous Silicon Thin Film MOS Transistors," The Transactions of The Institute of Electronics and Communication Engineers of Japan, Vol. J63-C No. 2, pp. 128-129, (Feb. 1980); Matsumura et al., "a-SI FET Switching Properties," National Convention Record, The Institute of Electronics and Communication Engineers of Japan, S3-12, pp. 2-285-286, (Mar. 1980); Spear et al., "Investigation of the Localized State Distribution in Amorphous Si Films," Journal of Non Crystalline Solids 8-10, pp. 727-738 (1972); and P. G. Le Comber, W. E. Spear, A. Ghaith, "Amorphous-Silicon Field-Effect Device and Possible Application," Electronics Letters, Vol. 15, No. 6, pp. 179-181 (Mar. 1979).

Because AU Optronics relies on the inventor's foregoing special definition of non-single crystal semiconductor, extrinsic evidence should not be permitted. Further, AU Optronics notes that in the September 11, 2002 Case Management Order, this Court has ordered, in relevant part in paragraph 4 concerning the claim construction hearing, that "[e]xpert testimony will normally not be needed but all sides may have an expert present to address points outside the intrinsic record should they arise." AU Optronics does not, therefore, identify any extrinsic evidence under Patent L.R. 4-2(b). However, if the Court decides to permit extrinsic evidence, AU

Optronics reserves the right to present extrinsic evidence concerning the phrase "non-single crystal semiconductor".

AU Optronics identifies the following term in asserted independent claims 3, 6, 10 and 11 and dependent claim 19 of the '941 patent for which it contends that construction by the Court is necessary:

". . . intrinsic . . ."

AU Optronics contends that the term "*intrinsic*" has a well-understood definition to those of ordinary skill in the relevant art, and that the term must be construed according to that definition so that "*intrinsic*" denotes a semiconductor "in which the concentration of charge carriers is characteristic of the material itself rather than of the content of impurities and structural defects of the crystal." *See* Exhibit C, p. 1 (McGraw Hill's Encyclopedia of Science and Technology on the Web, http://www.accessscience.com (hereinafter "McGraw Hill accessscience.com website"), search result under Dictionary Term option, entries for "intrinsic property" and "intrinsic semiconductor"); Exhibit D, p. 3 (McGraw Hill accessscience.com website, search result under Encyclopedia Article option, section entitled "Intrinsic semiconductors").

As additional examples of intrinsic evidence upon which AU Optronics may rely, AU Optronics cites the following from the prosecution history of the '941 patent: U.S. Patent Appl. Ser. No. 06/237,609, Application filed February 24, 1981, p. 9, l. 20 - p. 10, l. 3; *id.*, p. 12, ll. 14-18; *id.*, p. 16, l. 15 – p. 17, l. 8; *id.*, p. 26, l. 22- p. 27, l. 6; *id.*, p. 29, l. 10 - p . 30, l. 16; *id.*, p. 36; U.S. Patent Appl. Ser. No. 06/237,609, Amendment filed December 13, 1982, p. 4; U.S. Patent Appl. Ser. No. 06/278,418, Application filed June 29, 1981, p. 7, ll. 11-23; p. 9, l. 25 – p.

10, l. 25; p. 17, l. 13 – p. 18, l. 6; p. 21, ll. 2-18; p. 22, l. 10 – p. 24, l. 6; p. 27, l. 22 – p. 28, l. 5; Translation of Japanese Patent Application No. 55-088974, pp. 3, 4, 7-9, 10, 11-12, 14, 16-17; U.S. Patent Appl. Ser. No. 06/278,418, Amendment filed August 28, 1985, pp. 2-3, 5, 6; U.S. Patent Appl. Ser. No. 06/278,418, Amendment filed September 12, 1985, pp. 3, 4, 5; U.S. Patent Appl. Ser. No. 06/775,767, Amendment filed September 13, 1985, p. 5; U.S. Patent Appl. Ser. No. 07/488,102, Amendment filed March 28, 1991, pp. 1-5; U.S. Patent Appl. Ser. No. 07/488,102, Amendment filed May 2, 1991, pp. 2-11; U.S. Patent Appl. Ser. No. 07/602,167, Amendment filed October 23, 1990, pp. 1-2; U.S. Patent Appl. Ser. No. 07/602,167, Amendment filed May 2, 1991, pp. 4-9; U.S. Patent Appl. Ser. No. 07/602,167, Amendment filed December 12, 1991, pp. 7-11 and Appendices I & II; U.S. Patent Appl. Ser. No. 08/098,548, Amendment filed January 8, 1993, pp. 3-8; U.S. Patent Appl. Ser. No. 08/098,548, Declaration of Shunpei Yamazaki, dated January 21, 1993; U.S. Patent Appl. Ser. No. 08/098,548, Supplemental Response filed August 13, 1993, pp. 1-4; U.S. Patent Appl. Ser. No. 08/098,548, Amendment filed April 22, 1994, pp. 1-9; U.S. Patent Appl. Ser. No. 08/098,548, Office Action mailed July 14, 1994, pp. 2-5; U.S. Patent Appl. Ser. No. 08/098,548, paper no. 24, Interview Summary; U.S. Patent Appl. Ser. No. 08/098,548, Amendment filed December 2, 1994, pp. 2-13; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed January 11, 1995, pp. 2-13; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed June 21, 1995, pp. 1-16; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed October 10, 1995, pp. 12-13; U.S. Patent Appl. Serial No. 08/371,486, Supplemental Information Disclosure Statement and Response, filed October 17, 1995, pp. 1-4; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed May 29, 1996, pp. 8-14 and Appendix I; U.S. Patent Appl. Serial No. 08/371,486, paper no. 46, Interview Summary, Proposed Claims, pp. 9-11; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed July 31, 1996, pp. 13-15; U.S. Patent Appl. Serial No. 08/371,486, Declaration of Shunpei Yamazaki,

dated April 10, 1997; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed April 27, 1997, pp. 10-12, 18-21; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed January 22, 1998, pp. 1-3; U.S. Patent Appl. Serial No. 08/371,486, Appeal Brief filed April 16, 1998, pp. 4-5, 7, 8, 10-13, 15-17; and U.S. Patent No. 6,355,941, col. 3, ll. 23-36; col. 4, ll. 21-49; col. 7, ll. 10-28; col. 8, ll. 35-50; col. 9, ll. 1-47; col. 1, ll. 6-14.

As additional intrinsic evidence upon which AU Optronics may rely, AU Optronics cites the following references from the prosecution history files of the '941 patent: U.S. Patent No. 3,191,061; U.S. Patent No. 3,265,981; U.S. Patent No. 4,117,506; U.S. Patent No. 4,217,374; U.S. Patent No. 4,224,084; U.S. Patent No. 4,225,222; U.S. Patent No. 4,226,898; U.S. Patent No. 4,236,167; U.S. Patent No. 4,239,554; U.S. Patent No. 4,240,843; U.S. Patent No. 4,254,429; U.S. Patent No. 4,270,018; U.S. Patent No. 4,272,880; U.S. Patent No. 4,317,844; U.S. Patent No. 4,339,285; U.S. Patent No. 4,398,343; U.S. Patent No. 4,485,389; U.S. Patent No. 4,605,941; Translation of Published Japanese Patent Application No. 55-11329; Translation of Published Japanese Patent Application No. 55-11330; Translation of Published Japanese Patent Application No. 55-11330; Translation of Published Japanese Patent Application No. 55-11329; Translation of Published Japanese Patent Application No. 55-13938; Translation of Published Japanese Patent Application No. 55-13939; Japanese Published Patent Application No. 54-152894; Japanese Published Patent Application 55-050663; Japanese Published Patent Application 55-050664; S.M. Sze, Physics of Semiconductor Devices, pp. 568-621 (1969); W.E. Spear and P. G. Le Comber, "Electronic Properties of Substitutionally Doped Amorphous Si and Ge", Philosophical Magazine, 1976, vol. 33. N. 6, 935-949; M. Hirose, T. Suzuki, and G. H. Döhler, "Electronic Density of States in Discharge-Produced Amorphous Silicon," Applied Physics Letters, Vol. 34, No. 3, pp. 234-236 (Feb. 1, 1979); Nakamura et al., "Characteristics of Amorphous silicon TFTs," Extended Abstracts (The 40th Autumn Meeting), The Japan Society of Applied Physics, p. 325, 30P-S-17 (Sep. 1979); M. Hirose, T. Suzuki, and G. H. Doehler,

"Determination of Localized State Density Distribution in Glow Discharge Amorphous Silicon," Proceedings of the 10th Conference on Solid State Devices, JAP, vol. 18, pp. 109-113 (1979); Matsumura et al., "a-Si Thin Film MOS Transistor," Extended Abstracts (The 40th Autumn [sic?] Meeting), The Japan Society of Applied Physics, p. 326, 30P-S-18 (1979); Hiroshi Hayama and Masakiyo Matsumura, "Amorphous-Silicon Thin-Film Metal Oxide-Semiconductor Transistors," Applied Physics Letter, pp 754-755 (May 1980); M. Matsumura, "Amorphous Silicon Thin-Film Electro Devices," The Japan Society of Applied Physics, vol. 49, No. 7, pp 729(81)-732(84) (July 10, 1980); A. F. Tasch, Jr., T. C. Holloway, K. F. Lee, J. F. Gibbons, "Silicon-on-Insulator M.O.S.F.E.T.S. Fabricated on Laser-Annealed Polysilicon on SiO_2," Electronics Letters, Vol. 15, No. 14, pp. 435-437 (Jul. 1979); A. Matsuda et al., "Electrical and Structural Properties of Phosphorus-Doped Glow-discharge Si:F:H and Si:H Films" Japanese Journal of Applied Physics, vol. 19, No. 6, Jun., 1980, pp. L305-L308; A. Madan, P. G. Le Comber and W.E. Spear, "Investigation of the Density of Localized States in a-Si Using the Field Effect Technique," J. of Non-Crystalline Solids 20, pp. 239-257 (1976); Hiroshi Hayama and Masakiyo Matsumura, "a-Si FET IC Integrated on a Glass Substrate," National Convention Record, The Institute of Electronics and Communication Engineers of Japan, S3-13, pp. 2-287 to 2-288 (Mar. 1980); T. I. Kamins, "Field-Effects in Polycrystalline-Silicon Films," Solid-State Electronics, Vol. 15, pp 789-799 (Jul. 1972); S.M. Sze, Physics of Semiconductor Devices, p. 32 (1981); W. E. Spear and P. G. Le Comber, "Substitutional Doping of Amorphous Silicon," Solid State Communications, vol. 17, No. 9, pp. 1193-1196 (Nov. 1975); Hiroshi Hayama and Masakiyo Matsumura, "Amorphous Silicon Thin Film MOS Transistors," The Transactions of The Institute of Electronics and Communication Engineers of Japan, Vol. J63-C No. 2, pp. 128-129, (Feb. 1980); and P. G. Le Comber, W. E. Spear, A. Ghaith, "Amorphous-Silicon Field-Effect Device and Possible Application," Electronics Letters, Vol. 15, No. 6, pp. 179-181 (Mar. 1979).

Because AU Optronics relies on the customary and accepted definition of "intrinsic" to those of ordinary skill in the relevant art, and intrinsic evidence, extrinsic evidence should not be permitted. Further, AU Optronics notes that, in the September 11, 2002 Case Management Order, this Court has ordered, in relevant part in paragraph 4 concerning the claim construction hearing, that "[e]xpert testimony will normally not be needed but all sides may have an expert present to address points outside the intrinsic record should they arise." AU Optronics does not, therefore, identify any extrinsic evidence under Patent L.R. 4-2(b). AU Optronics nevertheless encloses the technical dictionary and encyclopedia source materials from which it read the ordinary and customary definition above, as it believes that such disclosures are consistent with the intent of Patent L.R. 4-2(b). *See Texas Digital Systems, Inc., v. Telegenix, Inc.*, 308 F.3d 1193, 1202-1203 (Fed. Cir. 2002) (dictionaries, encyclopedias and treatises are particularly useful resources, and may be the most meaningful sources of information, to assist the Court in determining the ordinary and customary meanings that would be attributed to claim-terms by those of ordinary skill in the relevant art). However, if the Court decides to permit extrinsic evidence, AU Optronics reserves the right to present extrinsic evidence concerning the term "intrinsic".

AU Optronics identifies the following term in asserted independent claims 3, 6, 10, 11, 12, 13, 14, 15, 16, 20 and 21 of the '941 patent for which it contends that construction by the Court is necessary:

". . . channel region . . ." or *". . . channel forming region . . ."*

AU Optronics contends that the term "*channel*" has a well-understood definition to those of ordinary skill in the relevant art, and that the term must be construed according to that

definition so that "*channel*" denotes "the main current path between the source and drain electrodes in a field-effect transistor or other semiconductor device." Because the channel of a field-effect transistor comes in and out of existence according to the charge applied to the transistor gate, it is appropriate to reference a channel region or channel forming region, which is that portion of the transistor where the channel forms. *See* Exhibit E, p. 1 (McGraw Hill accessscience.com website, search result under Dictionary Term option, entry 2 for "channel ... [ELECTRONICS]"); Exhibit F, pp. 5-7 (McGraw Hill accessscience.com website, search result under Encyclopedia Article option, section entitled "MOSFETs").

As additional examples of intrinsic evidence upon which AU Optronics may rely, AU Optronics cites the following from the prosecution history of the '941 patent: U.S. Patent Appl. Ser. No. 06/278,418, Application filed June 29, 1981, p. 29, ll. 5-18; Figs. 6D-6H; Translation of Japanese Patent Application No. 55-088974, p. 16; U.S. Patent Appl. Ser. No. 06/278,418, Amendment filed August 28, 1985, pp. 2-3, 5, 6; U.S. Patent Appl. Ser. No. 06/278,418, Amendment filed September 12, 1985, pp. 3, 4, 5; U.S. Patent Appl. Ser. No. 07/488,102, Amendment filed March 28, 1991, pp. 1-4; U.S. Patent Appl. Ser. No. 07/488,102, Amendment filed May 2, 1991, pp. 2-11; U.S. Patent Appl. Ser. No. 07/602,167, Amendment filed October 23, 1990, pp. 1-2; U.S. Patent Appl. Ser. No. 07/602,167, Amendment filed October 23, 1990, pp. 1-2; U.S. Patent Appl. Ser. No. 07/602,167, Amendment filed May 2, 1991, pp. 4-9; U.S. Patent Appl. Ser. No. 08/098,548, Amendment filed April 22, 1994, pp. 1-9; U.S. Patent Appl. Ser. No. 08/098,548, Office Action mailed July 14, 1994, pp. 2-5; U.S. Patent Appl. Ser. No. 08/098,548, paper no. 24, Interview Summary; U.S. Patent Appl. Ser. No. 08/098,548, Amendment filed December 2, 1994, pp. 2-13; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed January 11, 1995, pp. 2-13; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed June 21, 1995, pp. 1-16; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed October 10, 1995, pp. 12-13; U.S. Patent Appl. Serial No. 08/371,486,

Supplemental Information Disclosure Statement and Response, filed October 17, 1995, pp. 1-4; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed May 29, 1996, pp. 8-14 and Appendix I; U.S. Patent Appl. Serial No. 08/371,486, paper no. 46, Interview Summary, Proposed Claims, pp. 9-11; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed July 31, 1996, pp. 13-15; U.S. Patent Appl. Serial No. 08/371,486, Declaration of Shunpei Yamazaki, dated April 10, 1997; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed April 27, 1997, pp. 10-12, 18-21; U.S. Patent Appl. Serial No. 08/371,486, Amendment filed January 22, 1998, pp. 1-3; U.S. Patent Appl. Serial No. 08/371,486, Appeal Brief filed April 16, 1998, pp. 4-5, 7, 8, 10-13, 15-17; and U.S. Patent No. 6,355,941, col. 11, ll. 39-52; Figs. 6D-6H.

As additional intrinsic evidence upon which AU Optronics may rely, AU Optronics cites the following references from the prosecution history files of the '941 patent: U.S. Patent No. 3,191,061; U.S. Patent No. 3,265,981; U.S. Patent No. 3,339,128; U.S. Patent No. 3,999,212; U.S. Patent No. 4,236,167; U.S. Patent No. 4,272,880; Japanese Published Patent Application No. 54-152894; Japanese Published Patent Application 55-050663; Japanese Published Patent Application 55-050664; S.M. Sze, Physics of Semiconductor Devices, pp. 568-621 (1969); Nakamura et al., "Characteristics of Amorphous silicon TFTs," Extended Abstracts (The 40th Autumn Meeting), The Japan Society of Applied Physics, p. 325, 30P-S-17 (Sep. 1979); M. Hirose, T. Suzuki, and G. H. Doehler, "Determination of Localized State Density Distribution in Glow Discharge Amorphous Silicon," Proceedings of the 10th Conference on Solid State Devices, JAP, vol. 18, pp. 109-113 (1979); Matsumura et al., "a-Si Thin Film MOS Transistor," Extended Abstracts (The 40th Autumn [sic?] Meeting), The Japan Society of Applied Physics, p. 326, 30P-S-18 (1979); Hiroshi Hayama and Masakiyo Matsumura, "Amorphous-Silicon Thin-Film Metal Oxide-Semiconductor Transistors," Applied Physics Letter, pp 754-755 (May 1980); M. Matsumura, "Amorphous Silicon Thin-Film Electro Devices," The Japan Society of Applied Physics, vol. 49, No. 7, pp 729(81)-732(84) (July 10, 1980); A. Madan, P. G. Le

Comber and W.E. Spear, "Investigation of the Density of Localized States in a-Si Using the Field Effect Technique," J. of Non-Crystalline Solids 20, pp. 239-257 (1976); Hiroshi Hayama and Masakiyo Matsumura, "a-Si FET IC Integrated on a Glass Substrate," National Convention Record, The Institute of Electronics and Communication Engineers of Japan, S3-13, pp. 2-287 to 2-288 (Mar. 1980); T. I. Kamins, "Field-Effects in Polycrystalline-Silicon Films," Solid-State Electronics, Vol. 15, pp 789-799 (Jul. 1972); J. C. Anderson, "Localized States in the Mobility Gap of Amorphous Quartz and Glass," A Journal of Theoretical Experimental and Applied Physics, pp. 839-851 (Oct. 1974); Masakiyo Matsumura and Yasuo Nara, "a-Si P Channel FET," National Convention Record, The Institute of Electronics and Communication Engineers of Japan, pp. 2-281-282, S3-10 (Mar. 1980); M.J. Lee, "Preparation and Reliability of Thin Film Transistors Based on CdSe," Proc. 7th Intern. Vac. Congr. & 3rd Intern. Conf. Solid Surfaces, pp. 1979-1982 (Vienna 1977); Hiroshi Hayama and Masakiyo Matsumura, "Amorphous Silicon Thin Film MOS Transistors," The Transactions of The Institute of Electronics and Communication Engineers of Japan, Vol. J63-C No. 2, pp. 128-129, (Feb. 1980); Matsumura et al., "a-SI FET Switching Properties," National Convention Record, The Institute of Electronics and Communication Engineers of Japan, S3-12, pp. 2-285-286, (Mar. 1980); Spear et al., "Investigation of the Localized State Distribution in Amorphous Si Films," Journal of Non Crystalline Solids 8-10, pp. 727-738 (1972); and P. G. Le Comber, W. E. Spear, A. Ghaith, "Amorphous-Silicon Field-Effect Device and Possible Application," Electronics Letters, Vol. 15, No. 6, pp. 179-181 (Mar. 1979).

Because AU Optronics relies on the customary and accepted definition of "channel" to those of ordinary skill in the relevant art, and intrinsic evidence, extrinsic evidence should not be permitted. Further, AU Optronics notes that, in the September 11, 2002 Case Management Order, this Court has ordered, in relevant part in paragraph 4 concerning the claim construction hearing, that "[e]xpert testimony will normally not be needed but all sides may have an expert

present to address points outside the intrinsic record should they arise." AU Optronics does not, therefore, identify any extrinsic evidence under Patent L.R. 4-2(b). AU Optronics nevertheless encloses the technical dictionary and encyclopedia source materials from which it read the ordinary and customary definition above, as it believes that such disclosures are consistent with the intent of Patent L.R. 4-2(b). *See Texas Digital Systems, Inc.*, 308 F.3d at 1202-1203. However, if the Court decides to permit extrinsic evidence, AU Optronics reserves the right to present extrinsic evidence concerning the meaning of the phrase "channel region" or "channel forming region".

II. U.S. PATENT NO. 6,404,480

AU Optronics identifies the following term in asserted independent claims 1 and 11 of U.S. Patent No. 6,404,480 ("the '480 patent") for which it contends that construction by the Court is necessary:

". . . said second interlayer insulating film having at least two openings; . . . ."

AU Optronics contends that the proper claim construction of the foregoing element in independent claims 1 and 11 of the '480 patent is that the *"at least two openings"* in the second layer insulating film must all face the conductive spacers recited later in the same claims. Such a construction is essential to preserve the validity of these claims over prior art acknowledged in Figures 12-14 of the '480 patent and provided therein as part of the intrinsic evidence, namely plaintiff's Japanese patent application JP 9-094606 of March 27, 1997, relied on for foreign priority, including Figure 13 thereof.

As identification of the intrinsic evidence upon which AU Optronics relies in support of the foregoing construction, it identifies, in the patent prosecution file of the '480 patent, the

verified translation of Japanese Patent Application No. 9-094606, filed on March 27, 1997, and the Japanese patent application from which the translation was made. In particular, AU Optronics identifies the representation of the prior art in FIGS. 12-14 of the Japanese application attached to the verified translations and in the accompanying written description from page 7 of the verified translations, para. [0005] through page 8, para. [0011] showing two openings through the interlayer insulating film 18, namely (1) the opening by which the pixel electrode 19 is connected with the drain electrode of the TFT 17 and (2) the opening which receives the conducting panel 22.

Because AU Optronics relies on the intrinsic evidence, extrinsic evidence should not be permitted. Further, AU Optronics notes that, in the September 11, 2002 Case Management Order, this Court has ordered, in relevant part in paragraph 4 concerning the claim construction hearing, that "[e]xpert testimony will normally not be needed but all sides may have an expert present to address points outside the intrinsic record should they arise." AU Optronics does not, therefore, identify any extrinsic evidence under Patent L.R. 4-2(b). If, however, the Court decides to permit extrinsic evidence, AU Optronics reserves the right to present extrinsic evidence concerning the foregoing limitations.

III. U.S. PATENT NO. 5,929,527

AU Optronics identifies the following term in asserted independent claim 1 of U.S. Patent No. 5,929,527 ("the '527 patent") for which it contends that construction by the Court is necessary:

> *". . . the film made of aluminum or a material containing aluminum as a principal component contains oxygen atoms at a concentration of 8 x 10^{18} atoms $\bullet cm^{-3}$ or less, carbon atoms at a concentration of 5 x 10^{18} atoms $\bullet cm^{-3}$ or less, and nitrogen atoms at a concentration of 7 x 10^{17} atoms $\bullet cm10^{-3}$ or less."*

AU Optronics contends that each *"concentration"* recited above must be construed according to the inventor's special definition that "[t]he concentration of impurity elements is given by the ***maximum*** value measured by using SIMS (secondary ion mass spectroscopy)." This construction must be applied with regard to the further teaching that "[c]are should be taken in using SIMS for the measurement of the impurity concentrations, because a false value is sometimes measured in the vicinity of the interface of the film."

As the intrinsic evidence on which AU Optronics relies, it identifies the statements in the specification of the '527 patent at column 7, lines 63-65 and column 8, lines 8-11.

Because AU Optronics relies on the inventor's foregoing special definition of the concentration, extrinsic evidence should not be permitted. Further, AU Optronics notes that, in the September 11, 2002 Case Management Order, this Court has ordered, in relevant part in paragraph 4 concerning the claim construction hearing, that "[e]xpert testimony will normally not be needed but all sides may have an expert present to address points outside the intrinsic record should they arise." AU Optronics does not, therefore, identify any extrinsic evidence under Patent L.R. 4-2(b). If, however, the Court decides to permit extrinsic evidence, AU Optronics reserves the right to present extrinsic evidence concerning determination of concentration by SIMS.

IV. U.S. PATENT NO. 6,404,476

SEL, in its Patent L.R. 4-1 submission, has identified the following term in independent claims 6 and 22 of U.S. Patent No. 6,404,476 for which it contends that construction by the Court is necessary:

Claim 6: *wherein said conductive adhesive extends lengthwise beyond each end of the first and second electrodes.*

Claim 22: *each end of said first electrode and said second electrode is completely covered by said resin in a lengthwise direction.*

Claim 6: AU Optronics contends that the proper claim construction of the foregoing element of claim 6 is its literal meaning in which reference to "each end" of the electrode implies it has at least two ends. In particular, for the first electrode, which has two opposite ends as shown by element 9 in Figs. 2A and 2B of the patent, proper construction of this element of claim 6 requires that, at both ends, the conductive adhesive extend lengthwise beyond the end.

Claim 22: AU Optronics contends that the proper claim construction of the foregoing element of claim 22 is its literal meaning in which the word lengthwise denotes a direction along the length of the electrode. In particular, for the first electrode, this claim element of claim 22 requires that the first electrode must be covered by the resin along at least a portion that extends lengthwise, *i.e.*, for a distance that extends further in the direction of the length of the electrode than it extends in the direction of its width.

As the intrinsic evidence on which AU Optronics relies in support of the foregoing construction of claims 6 and 22, it identifies the language of claims 6 and 22 at column 6, lines 56-63, and column 8, lines 26-29, respectively. AU Optronics also relies upon the absence of any teaching contrary to the ordinary English meaning of the claim language in the specification, drawings or prosecution files.

AU Optronics contends that, since the literal meaning controls, and under Federal Circuit precedent, ordinary English dictionaries are intrinsic evidence, not extrinsic evidence (*see, e.g., Texas Digital Systems, Inc., supra*), extrinsic evidence should not be permitted.

Further, AU Optronics notes that, in the September 11, 2002 Case Management Order, this Court has ordered, in relevant part in paragraph 4 concerning the claim construction hearing, that "[e]xpert testimony will normally not be needed but all sides may have an expert present to address points outside the intrinsic record should they arise." AU Optronics does not, therefore, identify any extrinsic evidence under Patent L.R. 4-2(b). If, however, the Court decides to permit extrinsic evidence, AU Optronics reserves the right to present extrinsic evidence.

Dated: February 3, 2003

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Further, AU Optronics notes that, in the September 11, 2002 Case Management Order, this Court has ordered, in relevant part in paragraph 4 concerning the claim construction hearing, that "[e]xpert testimony will normally not be needed but all sides may have an expert present to address points outside the intrinsic record should they arise." AU Optronics does not, therefore, identify any extrinsic evidence under Patent L.R. 4-2(b). If, however, the Court decides to permit extrinsic evidence, AU Optronics reserves the right to present extrinsic evidence.

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EXHIBIT A

Exhibit A
Intrinsic Evidence for SEL's Claim Constructions

U.S. Patent 6,355,941

"non-single crystal semiconductor material"	
'941 Patent, Column 3, lines 37-40	"The non-single crystal semiconductor 7 means a semi-amorphous semiconductor, an amorphous semiconductor or a mixture thereof and it is desired to be the semi-amorphous semiconductor."
'941 Patent, Column 7, lines 29-36	"The above has clarified the manufacturing method of the present invention and its advantages in the case where the non-single crystal semiconductor 7 is the semi-amorphous semiconductor. Also in the case where the non-single crystal semiconductor 7 is an amorphous semiconductor or a mixture of the semi-amorphous semiconductor and the amorphous semiconductor, it can be formed by the above-described method, although no description will be repeated."
'941 Patent, Column 8, lines 25-30	"Even if the non-single crystal semiconductor 7 is the amorphous semiconductor or the mixture of the semi-amorphous and the amorphous semiconductor, the semi-amorphous semiconductor S2 is formed to have the same construction as in the case where the non-single crystal semiconductor 7 is the semi-amorphous one."
Prosecution History for U.S. Patent No. 5,091,334, Supplemental Amendment, May 2, 1991, Pg. 6	"In single crystalline or polycrystalline semiconductors, there is no lattice strain and thus the semiconductor of claims 21 and 29 excludes the fabrication of polycrystalline and moncrystalline semiconductors. Moreover, due to the random location of the atoms in amorphous semiconductor material, there is no lattice strain such materials and thus claims 21 and 29 also exclude the fabrication of amorphous semiconductors. Hence, claims 21 and [29] are directed to the fabrication of a semi-amorphous (SAS) semiconductor . . . ."
'941 Patent Prosecution History, Third Preliminary Amendment, May 2, 1991, Pgs. 4 - 5	"In single crystalline or polycrystalline semiconductors, there is no lattice strain and thus the semiconductor of claim 11 excludes polycrystalline and monocrystalline semiconductors. Moreover, due to the random location of the atoms in amorphous semiconductor material, there is no lattice strain in such materials and thus claim 11 also excludes amorphous semiconductors. Hence, claim 11 is directed to a semi-amorphous (SAS) semiconductor, which is characterized by a stable configurational state (see Fig. 5 of subject application) which occurs between the states associated with the amorphous and single crystalline (and polycrystalline states)."
'941 Patent Prosecution History, Examiner's Answer, August 24, 1998, Pgs. 3 - 4	"Matsumura does not explicitly state the use of recombination center neutralizer atoms, however, it was well known from Ovshinsky to practice these neutralizers with non-single crystal (amorphous) material to improve device function."

'941 Patent Prosecution History, Amendment, December 12, 1991, Pg. 8	"With respect to '938 or '939, both of them also fail to disclose semiconductor materials which comprise a mixture of crystalline and amorphous structures. Rather, they simply disclose the semiconductor materials are non-single crystalline, i.e. polycrystalline or amorphous. (In those applications, "non-single crystalline" is a generic term for polycrystalline structure and amorphous structures.)"

U.S. Patent 6,355,941

"channel region" or "channel forming region"	
'941 Patent, Column 11, lines 39-49	"The semiconductor device illustrated in FIG. 6H has a MIS type field effect transition structure which employs the regions 77 and 78 on the insulating substrate 62 as a source and a drain region, respectively, the region 79 as a channel region . . . . Since the regions 77, 78 and 79 serving as the source, the drain and the channel region have excellent properties as a semiconductor, the mechanism of an excellent MIS type field effect transistor can be obtained."
Figure 6H	See reference numeral 79 as described above.
'941 Patent Prosecution History, Amendment, December 2, 1994, Pg. 8	"Referring to the rejection of claims 29-41, 51-61, 71, and 72 under 35 U.S.C. 103 over Dill '981 in view of Weimer '061, the present invention is characterized by a semiconductor device having a non-doped non-single silicon as a channel region extending between source and drain regions which comprise impurity doped non-single crystalline silicon."
'941 Patent Prosecution History, Amendment and Information Disclosure Statement, June 21, 1995, Pgs. 10-11	"As discussed in the Amendment of December 2, 1994, the present invention is characterized by a semiconductor device having an intrinsic or substantially intrinsic, non-single crystalline silicon as a channel region extending between source and drain regions which comprise impurity doped non-single crystalline silicon."

U.S. Patent 6,355,941

"intrinsic"	
Patent Prosecution History for U.S. Application No. 06/775,767, Office Action, July 22, 1986, Pg. 2	"In claim 23, line 13 'having I conductivity type, is inappropriate since 'I' means intrinsic or 'undoped'."
'941 Patent Prosecution History, Amendment, December 2, 1994, Pgs. 8-9	"Typically, the channel region is a I type layer while source and drain regions are N or P type. Thus, the characterizing feature of the channel of the semiconductor device of the present invention is that it is (a) non-single crystalline and (b) non-doped."

'941 Patent Prosecution History, Declaration under 37 C.F.R. 1.132, January 21, 1993, Pg. 2	"It should be noted that any impurity which renders the silicon p-type or n-type was not intentionally added in order that the deposited silicon is of intrinsic conductivity type."
JP Patent Application No. 53-83467, Pg. 6 (translation)	"When impurities such as phosphorus, arsenic, which provide N-conductivity type in a semiconductor, are mixed in the non-single-crystalline film . . . the so-called N-type semiconductors are produced. On the other hand, when diborane . . . is added at the same concentration, P-type semiconductors are produced. Furthermore, when no impurities whatsoever are added, the intrinsic or so-called substantially intrinsic semiconductors with the inclusion of background level impurities is obtained. In addition . . . hydrogen, deuterium, or a halogen compound such as chlorine is added to this non-single-crystalline film . . . ."
JP Patent Application No. 53-83467, Pg. 10 (translation)	"The semiconductor 26 and 27 are intrinsic or substantially intrinsic in light, although 26 has more additives than 27. 27 has a 1-5% nitrogen atomic concentration, 26 has 3-10%, and 25 has 5-30%."
'941 Patent Prosecution History, Amendment and Information Disclosure Statement, June 21, 1995, Pg. 11	"Typically, the channel region is I type while the source and drain regions are both N type or both P type. Thus, the characterizing feature of the channel of the semiconductor device of the present invention is that it is (a) non-single crystalline and (b) intrinsic or substantially intrinsic."
'941 Patent Prosecution History, Office Action, July 14, 1994, Pg.3	"Dill teaches a thin film transistor with a 'substantially intrinsic' or 'non-doped' channel region."
'941 Patent Prosecution History, Appeal Brief, April 16, 1998, Pg. 7	"From the Office Action mailed June 14, 1996, the examiner appears to rely on Matsumura for the teaching of a thin film FET including an undoped or intrinsic channel region and n+ doped source and drain regions."
'941 Patent Prosecution History, Office Action, January 26, 1996, Pgs. 3-4	"The prior art teaches doped source and drain regions, silicon nitride gate insulating film, and intrinsic or undoped channel regions in thin film structure."

U.S. Patent 5,929,527

"The film made of aluminum or a material containing aluminum as a principal component contains oxygen atoms at a concentration of $8x10^{18}$ atoms·cm^{-3} or less, carbon atoms at a concentration of $5x10^{18}$ atoms·cm^{-3} or less and nitrogen atoms at a concentration of $7x10^{17}$ atoms·cm^{-3} or less"	
'527 Patent, Column 1, lines 56-65	"According to one constitution of the present invention, there is provided an electronic device characterized in that it comprises a film pattern made of aluminum or a material containing aluminum as the principal component thereof, wherein the film made of aluminum or a material containing aluminum as the principal component contains oxygen atoms at a concentration of $8x10^{18}$ atoms·cm^{-3} or less, carbon atoms at a concentration of $5x10^{18}$ atoms·cm^{-3} or less, and nitrogen atoms at a concentration of $7x10^{17}$ atoms·cm^{-3} or less."
'527 Patent, Column 7, lines 62-64	"The concentration of impurity elements [given in Table 1] is given by the maximum value measured by using SIMS (secondary ion mass spectroscopy)."
'527 Patent, Column 8, lines 8-11	"Care should be taken in using SIMS for the measurement of the impurity concentration, because a false value is sometimes measured in the vicinity of the interface of the film."

U.S. Patent 6,404,476

"wherein said conductive adhesive extends lengthwise beyond each end of the first and second electrodes" and **"each end of said first electrode and said second electrode is completely covered by said resin in a lengthwise direction"**	
'476 Patent Prosecution History, Amendment, December 2, 1999, page 4	"Independent claim 23 has been amended to recite that an end of the electrodes is completely covered by the conductive paste. That is, the conductive paste extends beyond an end of the electrodes. Please see Fig. 3 of the present application in this regard. This feature is advantageous to improve the reliability of the electrical and mechanical connection between the two parts, i.e., the first and second electrodes. Specifically, since the end of the electrodes is completely covered by a resin, it is possible to avoid problems caused by moisture."
'476 Patent Prosecution History, Amendment, December 2, 1999, page 2	"wherein said conductive adhesive extends beyond each end of said first and second electrodes"
'476 Patent Prosecution History, December 2, 1999, page 3	"and each end of said first electrode and said second electrode is completely covered by said resin"
'476 Patent Prosecution History, After Final Amendment, July 3, 2000, page 2	"an electrically conductive adhesive, through which said first and second electrodes are connected to each other, wherein said conductive adhesive extends lengthwise beyond each end of the first and second electrodes"
'476 Patent Prosecution History, After Final Amendment, July 3, 2000, page 2	"wherein each of said conductive particles comprises a resilient particle coated with a metal film, and each end of said first electrode and said second electrode is completely covered by said resin in a lengthwise direction."
'476 Patent Prosecution History, After Final Amendment, July 3, 2000, page 3	"The present invention, as currently set forth in independent claims 23 and 47 and illustrated in Fig. 3, for example, discloses an adhesive that overlaps, in a lengthwise direction electrode strips 9 located on opposing substrates 1. In the Official Action, Tsukagoshi document is utilized to teach the use of resilient conductive particles and spacer particles. As illustrated in Fig. 3 of Tsukagoshi, this reference illustrates a cross-sectional view of connected conductors. Adhesive 4 enables electroconductive adhesion between conductors 5 and 6."
'476 Patent Prosecution History, After Final Amendment, July 3, 2000, pages 3-4	"Turning to the claims, Applicant respectfully submits that Tsukagoshi does <u>not</u> disclose an electrically conductive adhesive, through which said first and second electrodes are connected to each other, wherein said conductive adhesive extends <u>lengthwise</u> beyond each end of the first and second electrodes as now recited in claim 23, or that each end of said first electrode and said second electrode is completely covered by said resin <u>in a lengthwise direction</u>, as now recited in claim 47."

U.S. Patent No. 4,999,460 to Sugiyama et al.,	Figs. 1 and 8
'476 Patent Prosecution History, Response, June 20, 2001	"With respect to claim rejections, Applicant will submit a verified English Translation of the Japanese priority document in order to overcome the outstanding rejections based on Sugiyama et al. The filing date of the Japanese Priority Application is September 1, 1989, while Sugiyama et al. was filed November 6, 1989. Thus, Sugiyama et al. is not prior art."
Japanese Priority Document No. 1-232308	Fig. 2
'476 Patent	Fig. 3
'476 Patent, Column 2, lines 42-44	"Fig. 3 is a partial cross-sectional view showing electrical connection between substrates carrying electrode strips in accordance with the present invention."
'476 Patent, Column 2, lines 64-67	"The auxiliary substrates 3 and the substrates 1 and 2 are connected respectively at their edges in order to establish electrical coupling between corresponding electrodes."
'476 Patent, Column 3, lines 38-43	"One side of each of the first and second substrates extends together with the electrode strips and is exposed beyond the other substrate in order to provide contacts for electrically connection with the driving circuits formed on the auxiliary substrates 3 as shown in Fig. 1."
'476 Patent, Column 3, lines 62-67, Column 4, lines 1-14	"The electric connection between the first and second substrates 1 and 2 and the counterpart auxiliary substrates 3 respectively are done as follows. The extended inside surfaces of the first substrates 1 on which terminals of the respective electrodes are exposed are coated, by means of a dispenser, with an anisotropic conductive film. The adhesive film is made from a UV light curable adhesive 8 in which a number of resilient fine conductive particles 6 and hard particles 7 whose diameter is slightly smaller than that of the resilient particles are dispersed. The resilient particles are made from 7.5 μm thick polystyrene spheres plated with a 1000 angstroms thick Au film. The hard particles are made from 5 μm thick SiO_2 spheres. The weight proportion among the adhesive, the resilient particles and the hard particles is 107:14:1. Then, the first substrate 1 and the auxiliary substrates 3 are joined with the adhesive therebetween in order that the the terminals of the first substrate 1 and the corresponding contacts of the auxiliary substrate 3 are aligned to each other, and exposed to UV light for 3 minutes under pressure of about 2.4 kg/cm^2."

'476 Patent, Column 4, lines 47-66	"The electric connection between the first and second substrates 1 and 2 and the counterpart auxiliary substrates 3 respectively are done as follows. The extended inside surfaces of the first substrates 1 on which terminals of the respective electrodes are exposed are coated, by means of a dispenser, with an anisotropic conductive film. The adhesive film is made from a UV light curable adhesive 8 in which a number of resilient fine conductive particles 6 and hard particles 7 whose diameter is slightly smaller than that of the resilient particles are dispersed. The resilient particles are made from 2.5 μm thick polystylene [*sic*: polystyrene] spheres plated with a 1000 angstroms thick Au film. The hard particles are made from 2 μm thick SiO_2 spheres. The weight proportion among the adhesive, the resilient particles and the hard particles is 98:13:3. Then, the first substrate 1 and the auxiliary substrates 3 are joined with the adhesive therebetween in order that the the [*sic*] terminals of the first substrate 1 and the corresponding contacts of the auxiliary substrate 3 are aligned to each other, and exposed to UV light for 3 minutes under pressure of about 2.4 kg/cm^2."
'476 Patent, Column 5, lines 33-40	"One side of each of the first and second substrates extends together with the electrode strips and is exposed beyond the other substrate in order to provide contacts for electrically connection with the driving circuits formed on the auxiliary substrates 3 as shown in FIG. 1. Then, a pair of auxiliary substrates are provided, tested and coupled with the liquid crystal panel in the same manner as the above embodiment."

U. S. Patent 6,404,480

"Second interlayer insulating film having at least two openings"	
'480 Patent, Abstract, lines 9-11	"Openings are formed in the dielectric film. A second conducting film covers the dielectric film left and the openings."
'480 Patent, Column 2, lines 30-58	"In the prior art liquid crystal display, the interlayer dielectric film 18 is provided with the opening at the common contact portion 16, as shown in FIG. 13. Therefore, the cell gap G_c in the common contact portion is almost equal to the sum of the cell gap G_p in the pixel region+the film thickness t of the interlayer dielectric film 18. "The cell gap G_p (also known as the cell spacing) in the pixel region 12 is determined by the insulating spacers 25. It is common practice to use standardized spacers as the insulating spacers 25 and so if the spacers 25 have a uniform diameter, the cell gap G_p in the pixel region 12 is substantially uniform among liquid-crystal cells. However, it is difficult to avoid nonuniformity of the cell gap G_c in the common contact portion among liquid-crystal cells. "The cell gap G_p in the common contact portion is constant since the cell gap G_p is constant because of the relation described above. Therefore, the cell gap G_c in the common contact portion depends only on the film thickness t of the interlayer dielectric film 18. Consequently, to make the cell gap G_c uniform among liquid-crystal cells, it is necessary that the film thickness t of this interlayer dielectric film 18 be uniform among cells. However, this is impossible to circumvent. "Normally, the common contact portions of the liquid crystal display are 2 to 4 in number. The film thickness t of the interlayer dielectric film 18 may differ from location to location on the same substrate. In this case, the film thickness t may differ among different common contacts even on the same substrate. "Because of the aforementioned nonuniformity of the thickness t of the interlayer dielectric film 18, the cell gap G_c in the common contact portion differs among different cells or different common contacts. Furthermore, the nonuniformity of the cell gap G_c results in the cell gap G_p in the pixel region to be nonuniform."
'480 Patent, Column 3, lines 22-28	"It is an object of the present invention to provide a contact structure which is free of the foregoing problems, provides less nonuniform cell gap among different cells if the thickness of the interlayer dielectric film is nonuniform across the cell or among different cells, and reduces poor electrical contacts which would normally be caused by conducting spacers."

'480 Patent, Column 3 lines 29-44	"This object is achieved in accordance with the teachings of the invention by a contact structure for connecting a conducting film formed on a first substrate with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film to expose parts of the first conducting film by selectively leaving the dielectric film; a second conducting film covering the dielectric film left and the openings; a third conducting film formed on the second substrate; and conducting spacers held between the first and second substrates and connecting the second and third conducting films. The second conducting film is connected with the first conducting film through the openings."
'480 Patent, Column 3 lines 49-65	"One embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film to expose parts of the first conducting film; an insulator deposited on only portions of the first conducting film exposed through the openings; a second conducting film covering the openings; a third conducting film formed on the second substrate; and conducting spacers held between the first and second substrates and connecting the second and third conducting films. The second conducting film is connected with the first conducting film through the openings extending through the insulator."
'480 Patent, Column 4, lines 3-20	"Another embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate of an electrooptical device with a counter electrode formed on a second substrate opposite to the first substrate, which has pixel electrodes formed thereover, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate and under the pixel electrodes; an interlayer dielectric film covering the first conducting film; openings formed in the interlayer dielectric film to expose parts of the first conducting film by selectively leaving the interlayer dielectric film;a second conducting film defining the counter electrode formed on the second substrate; a third conducting film covering the interlayer dielectric film left and the openings; and conducting spacers held between the first and second substrates and connecting the second and third conducting films. The second conducting film is connected with the first conducting film through the openings."

'480 Patent, Column 4 lines 27-47	"A further embodiment of the invention resides in a contact structure for connecting a first conducting film formed over a first substrate of an electrooptical device with a counter electrode formed on a second substrate opposite to the first substrate, which has pixel electrodes formed thereon, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate and under the pixel electrodes; an interlayer dielectric film covering the first conducting film; openings formed in the interlayer dielectric film to expose parts of the first conducting film; an insulator formed on selected portions of the surface of the first conducting film extending through the openings; a second conducting film covering the openings; a third conducting film defining the counter electrode formed on the second substrate; conducting spacers held between the first and second substrates and connecting the second and third conducting films. The pixel electrodes and the second conducting film are formed from a common starting film. The second conducting film is connected with the first conducting film through the openings extending through the insulator."
'480 Patent, Column 4 line 52 – Column 5 line 2	"A still other embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film and exposing parts of the first conducting film; a second conducting film covering the openings; a third conducting film formed over the second substrate; a fourth conducting film formed between the second substrate and the third conducting film and in contact with the third conducting film; and conducting spacers held between the first and second substrates. The first conducting film, the second conducting film, the conducting spacers, the third conducting film, and the fourth conducting films are connected in turn through the openings. The spacers maintain the cell gap between the first and second substrates."
'480 Patent, Column 5 lines 66-67	"In the present embodiment, openings are formed, selectively leaving the interlayer dielectric film 18."
'480 Patent, Column 6 lines 4-8	"The dielectric film 104 is selectively left to form openings 111 that expose parts of the first conducting film 103. A second conducting film 105 is formed so as to cover the left parts of the dielectric film, 104a, and the openings 111."
'480 Patent, Column 6 lines 12-18	"In the present embodiment, the dielectric film 104 is selectively left to form the dielectric film portions 104a and the openings 111. The openings 111 expose parts of the first conducting film 103. The first conducting film 103 is connected with the second conducting film 105 at these openings 111."

'480 Patent, Column 6 lines 34-39	"In the present embodiment, it is desired that the area of each opening 111 be sufficiently larger than the area occupied by each conducting spacer and offer space so that the conducting spacers can move freely, because the spacers 107 existing in the openings 111 do not contribute toward maintaining the gap."
'480 Patent, Column 6 line 51-52	"The openings 111 are formed as shown in FIG. 2A in the present embodiment."
'480 Patent, Column 7 lines 2-3	"The present embodiment is characterized in that the dielectric film 18 is selectively left to form openings."
'480 Patent, Column 7 lines 12-14	"The dielectric film 104 is provided with openings 111 to selectively expose the surface of the first conducting film 103."
'480 Patent, Column 7 lines 15-16	"A second conducting film 105 is formed to cover the openings 111."
'480 Patent, Column 9 lines 60-64	"Contact holes for gaining access to the source and drain regions 310 and 311, respectively, were created in the first interlayer dielectric film 315. Contact holes for allowing access to the internal conducting lines 207c were formed in the common contact portions 206c and 206d."
'480 Patent, Column 10 lines 24-36	"Then, contact holes 320 and 321 were formed in the second interlayer dielectric film 319 to have access to the drain electrode 317 and to the internal conducting lines 318, respectively. The contact holes 321 for the internal conducting lines 318 were formed in the openings 111 shown in FIG. 2A. That is, rectangular holes measuring 100 μm x 100μm were arranged in 5 rows and 5 columns within the rectangular region 110 measuring 1.1 mm x 1.1 mm. These holes were spaced 100 μm from each other. Moreover, the contact holes for connecting the internal conducting lines 318 (207a and 207b) with the common terminals 205a and 205b at the extractor terminals 205 were formed. "
'480 Patent, Column 10 lines 37-39	"As described later, the size of each hole was set to 100 μm x 100 μm to set the diameter of the conducting spacers to 3.5μm in this example."
'480 Patent, Column 10 lines 56-58	"This pad 323 measured 1.1 mm x 1.1 mm, was rectangular, and covered the contact holes 321."
'480 Patent	Figures 1, 2A, 5F, 5G, 6, 7, 8, 9, 10

Extrinsic Evidence for SEL's Claim Constructions

U.S. Patent 6,355,941

"intrinsic"
Nakano, Shoichi, *et al.*, "High Performance a-Si Solar Cells and Narrow Bandgap Materials," Mat. Res. Soc. Symp. Proc. Vol. 49 (1985)
Kaneko, S., *et al.*, "Amorphous Si:H Heterojunction Photodiode and its Application to a Compact Scanner," Mat. Res. Soc. Symp. Proc. Vol. 49 (1985)
Suzuki, Kouji, *et al.*, "14.2/9:25 A.M.: High-Resolution Transparent-Type a-Si TFT LCDs," 146 SID 83 Digest (1983)
Nagayasu, T., *et al.*, "1988 International Display Research Conference – A 14-in.-Diagonal Full-Color a-Si TFT LCD" (1988)
Ichikawa, K., *et al.*, "14.1: 14.3-in.-Diagonal 16-Color TFT-LCD Panel Using a Si:H TFTs," 226 SID 89 Digest (1989)
Martin, Russel A., *et al.*, "High Voltage Amorphous Silicon Thin-Film Transistors," IEEE Transactions on Electron Devices, Vol. 40, No. 3 (1993)

EXHIBIT B

EXHIBIT B

SEL'S EXPERT WITNESSES FOR CLAIM CONSTRUCTION HEARING

1) PAUL A. KOHL, Ph.D.

2) L. RAFAEL REIF, Ph.D.

Curriculum Vitae

Paul A. Kohl, Ph.D.

PROFESSIONAL EXPERIENCE

1989 to Present	**Georgia Institute of Technology**	
	1999 to Present	**Regents Professor**
	1994 to 1999	**Professor**
	1989 to 1994	**Associate Professor**
1978 to 1989	**AT&T Bell Laboratories**	
	1982 to 1989	**Technical Supervisor**
	1978 to 1982	**Member of Technical Staff**

CURRENT RESEARCH PROJECTS

1. *Electronic Packaging:* Director of materials and processing research for NSF Center of Excellence in Electronic Packaging at Georgia Tech. Current project include design of advanced packaging structures, rapid processing methods, and novel interconnection materials. Courses developed and taught include Ch.E./E.C.E 4803 Fabrication of advanced printed circuit boards.

2. *Interconnects for Future Integrated Curcuits:* Director of Research for the Georgia Tech portion of the Interconnect Focus Center (IFC), sponsored by the SIA (via MARCO), and DARPA. The IFC is housed at Georgia Tech with contributions from other universities. The focus of the work is advanced interconnection and assembly of integrated circuits. Courses developed and taught include Ch.E./E.C.E. 4752 CMOS integrated circuit fabrication laboratory course, and Ch.E. 4400 Chemical and Process Safety.

3. *Power Sources for Integrated Curcuits:* The integration of microfuel cells into integrated circuits for on-board power.

4. *Insulators for Integrated Circuits:* Ultra low dielectric constant insulators for integrated circuit and printed wiring board uses.

5. *Novel Uses of IC Technology:* Microfluidic devices on silicon for lab-on-a-chip applications sponsored by NSF.

6. *Low Temperature Molten Salts- Electrodeposition and Batteries:* New room temperature ionic liquids are promising electrolytes for deposition of metals for producing novel deposits and high energy density batteries, sponsored by the Department of Energy.

PREVIOUS RESEARCH PROJECTS AT BELL LABORATORIES

1. *New Chemical Processes for the Manufacture of Printed Wiring Boards.* This includes the development and implementation of high speed solder, gold, and copper processes, and the reduction in the use and discharge of chemicals.
2. *Integrated Electrical and Optoelectronic Devices:* This includes the invention of new manufacturing methods for the production of integrated devices into field effect transistors, and optoelectronic devices.
3. *Thin Film Analysis Laboratory:* Formed and staffed a state-of-the-art analytical laboratory of the characterization and analysis of thin films for the development of next generation silicon and compound semiconductor devices.
4. *Silicon-on-Silicon Electronic Packaging*: Lead a research and development group for ultra high density packaging of CMOS silicon devices. The includes the operation of a prototype manufacturing facility.
5. *CMOS Device Development Laboratory*: Responsible for the 0.9 μm CMOS device development line where new processes and products were investigated.

OTHER PROFESSIONAL EXPERIENCE

Consulting Experience

- AT&T Bell Laboratories (1989-1991): Fabrication of multi-chip modules (electronic packaging) for advanced VLSI.
- N-Chip Inc. (1990-1992): Processing of multi-chip modules.
- Bell South, high capacity power sources.
- Curry Manufacturing (1993-1995): Design and fabrication of electroluminescent devices.
- Superior Teletec (1993-1995): Fabrication of advanced electronic displays- product evaluation.
- BFGoodrich (1993-present): Synthesis of microelectronic polymer materials.
- Amoco Performance Products (1994-1997): Microelectronic uses of polymers and carbon fibers.
- Lester Manufacturing (1996-1999): Chemicals used in consumer products.
- 3M (1997-present): Chemical mechanism for the Simons process (synthesis of perfluorination).
- Sachem (1998-present): The use of quaternary amines in microelectronics.

- Emissarius Ltd. (1998-present): Marketing of polymers in Microelectronics.

EDUCATION

Ph.D., Chemistry (Electrochemistry), University of Texas at Austin, 1978
BS, Chemistry, Bethany College, 1974

PATENTS

Patent Number	Year Issued	Title
6,165,890	2000	Fabrication of a Semiconductor Device with Air Gaps for Ultra-Low Capacitance Interconnections
6,162,838	2000	Porous Insulating Compounds and Method for Making Same
6,141,072	2000	System and Method for Efficient Manufacturing of Liquid Crystal Displays
5,468,688	1995	Process for the Low Temperature Creation of Nitride Films on Semiconductors
5,348,627	1994	Process and System for the Photoelectrochemical Etching of Silicon in an Anhydrous Environment
4,689,125	1987	Fabrication of Cleaved Semiconductor Lasers
4,622,114	1986	Process of Producing Devices with Photoelectrochemically Produced Gratings
4,576,691	1986	Etching Optical surfaces on GaAs
4,482,443	1984	Photoelectrochemical Etching of n-type Si
4,482,442	1984	Photoelectrochemical Etching of n-Type Gallium Arsenide

4,425, 196	1984	Photoelectrochemical Plating of Silver
4,415,414	1983	Etching of Optical surfaces
4,414,066	1983	Electrochemical Photoetching of Compound Semiconductors
4,404,072	1983	Photoelectrochemical of Processing III-V Semiconductors
4,399,004	1983	Photoelectrochemical Gold Plating Process
4,389,291	1983	Photoelectrochemical Processing of InP Type Devices
4,379,738	1983	Electro Plating Zinc
4,377,449	1983	Electrolytic Silver Plating
4,377,448	1983	Electrolytic Gold Plating
4,376,018	1983	Electrodeposition of nickel
4,369,099	1983	Photoelectrochemical Etching of Semiconductors
4,310,392	1982	Electrolytic Plating
4,263,106	1981	Solder Plating Process
4,236,976	1980	Preventing Stains on Multiple-Electroplated Articles
4,229,269	1980	Spray Cell for Selective Metal Deposition or Removal

PROFESSIONAL AFFILIATIONS & AWARDS

Editorial Service

Editor-in-Chief, *Journal of The Electrochemical Society*, 1995-present

Editor-in-Chief (Founding Editor), *Electrochemical and Solid-State Letters*, 1998-present

Editor (Founding Editor), The Electrochemical Society Interface, 1992-1995

Affiliations
Member, Electrochemical Society
Member, American Institute of Chemical Engineers (AICHE)
Member, American Chemical Society
Member, Materials Research Society

Honors and Awards

Carl Wagner Memorial Award, The Electrochemical Society, 2001
Research Award: NSF-ERC in Electronic Packaging, 1999.
Research Program Development Award, 1995, Georgia Tech.
Named Institute Fellow, 1994, Georgia Tech.
Outstanding Faculty Award, 1990-1991, Chemical Engineering, Georgia Tech.
Outstanding Faculty Award, 1990-1991, AICHE Student Chapter Georgia Tech.
Outstanding Alumni Achievement Award presented by Bethany College in 1986.
Named one of "America's 100 Brightest Scientists Under 40" by Science Digest in 1985.
Edward Weston Fellowship from the Electrochemical Society in 1977.
Gilbert H. Ayers for outstanding graduate work in chemistry in 1977.
Awarded Academic Distinction in chemistry from Bethany College in 1974.
Analytical Chemistry Award from the American Chemical Society in 1973.

PUBLICATIONS

Refereed Journal Papers

1. Kohl, P.A., and Bard, A.J., "The Characterization and Behavior of n-Type ZnO, CdS and GaP Electrodes in Acetonitrile Solutions," *Journal of the American Chemical Society, 99*, 7531-7539 (1977).

2. Kohl, P.A., Frank, S.N., and Bard, A.J., "Behavior of n- and p-Type single Crystal Semiconductors Covered with Thin n-TiO_2 Films," *Journal of the Electrochemical Society, 124*, 225-229 (1977).

3. Noufi, R.N., Kohl, P.A. and Bard, A.J., "Electrochemistry and Electroluminescence at n-Type TiO_2 in Aqueous Solutions," *Journal of the Electrochemical Society, 125*, 246-252 (1978).

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Presentations

Conference Presentations with Proceedings (refereed)

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20. Kohl, P.A., "Metallurgy and Processing for Advanced Mixed Mode Electronic Packaging," Invited presentation to the Defense Sciences research Council, July 8, 1993.

21. Twyford, E.J., Kohl, P.A., Jokerst, N.M., Hartman, N.F., "The Resolution of Holographic Etching of Gratings," The Electrochemical Society, Phoenix, AZ, October 1991.

22. Propst, E., Harris, D.B., and Kohl, P.A., "The Photoelectrochemical Etching of n-GaSb and n-InAs," The Electrochemical Society, Phoenix AZ, 1991.

23. Vogt, K., and Kohl, P.A., "Low Temperature Chemical Vapor Deposition of Group III and Transition Metal Nitride Films," American Institute of Chemical Engineers National Meeting, November 1992.

24. Gray, G.E., Winnick, J., and Kohl, P.A., "A Room Temperature Molten Salt Electrolyte For The Sodium/Iron Chloride Battery" *IECEC Energy Conversion Engineering Conference, 44*, 1139, Atlanta, GA, August 1993.

25. Frye, D.C., Harris, R.H., Heistrand, R.H., Moyer, E.S., Rutter, E.W., Garrou, P., Berry, M.J., Rogers, B., Turlik, I., Bidstrup, S.A., Hodge, T., Kohl, P.A., Taylor, G., Berry, K., David, F., and Lanka, M., "Via Generation in Cytclotene," VLSI Packaging, Kyoto, Japan December 2, 1992.

26. Hodge, T., Bidstrup, S.A., and Kohl, P.A., "The Effect of Moisture and Temperature on the Dielectric Properties of Polyimides," *The Electrochemical Society*, vol. 93-12, 451-2, St. Louis, MO, October 1992.

27. Han, S.S., Ceiler, M., Bidstrup, S.A., Kohl, P.A., May, G., "Em,perical Modeling of Plasma Enhanced CVD of Silicon Dioxide Using Neural Networks," SPIE Conf. on Microelectronics, Monterey, CA, Sept. 1993.

28. Hodge, T.C., Kohl, P.A., Bidstrup, S.A., Lee, J.B., Allen, M.G., "An In-Situ Measurement Technique for Through-Plane Thermal Properties of Thin Films," AICHE, St. Louis, MO, November 11, 1993.

29. Sullivan, A., Patel, A.J., and Kohl, P.A. "Low pH Electroless Gold," Plating and Surface Finishing, April 1994.

30. Sullivan, A., Patel, A.J., and Kohl, P.A. "Low pH Electroless Gold Deposition from Gold Thiosulphate," Electrochemical Society, Sam Francisco, CA, May 1994.

31. Kokan, J.R., Tadayon, F., Gerhardt, R., and Kohl, P.A. "Sol-Gel Processing of Porous Silica Thin Films," 98th Meeting of the American Ceramic Society, Indianapolis, Indiana, 1994.

32. Gray, G., Kohl, P.A., and Winnick, J., "Room Temperature Molten Salt Battery," The Electrochemical Society, Miami, FL, October 1994.

33. Rieger, M.M., Kohl, P.A., "Luminescence of Porous Silicon Formed in Acetonitrile," The Electrochemical Society, Miami, FL, October 1994.

34. K, J., Gerhardt, R., and Kohl, P.A., "Porous Silica," NATO conference, 1994.

35. Stalder, S.M., Ding, Y., Sturrock, P.E., Winnick, J., Kohl, P.A., and Bottomley, L.A., "A Continuous On-line Process Stream Monitor for the Electrolytic Production of Sodium Hydrosulfite," American Chemical Society, Analytical Chemistry Division, 1994.

36. Rieger, M.M., and Kohl, P.A., "Formation of Porous Silicon," Materials Research Society, Boston, MA, November 1994.

37. Pye, S.L., Winnick, J., and Kohl, P.A., "The Electrochemical Behavior of Copper and Nickel Electrodes in Sodium Chloride Buffered, Neutral Room Temperature Aluminum Chloride 1-Methyl-3-Ethyl Imidazolium Chloride Molten Salt," 189th Meeting of the Electrochemical Society, Los Angeles, CA, May 1996.

38. Pye, S.L., Gray, G.E., Winnick, J., and Kohl, P.A., "Room Temperature Molten Salts: Applications as Battery Electrolytes," 189th Meeting of the Electrochemical Society, Los Angeles, CA, May 1996.

39. Gray, G.E., Winnick, J., and Kohl, P.A., "Comparisons of the Plating and Stripping of Sodium from Room Temperature Molten Salts," 189th Meeting of the Electrochemical Society, Los Angeles, CA, May 1996.

40. Rieger, M.M., Flake, J., and Kohl, P.A., "A Photoelectrochemical Process for Fabricating Three--Dimensional Structures in Silicon," AIChE, November 1996.

41. Rieger, M.M., Flake, J., and Kohl, P.A., "The Elimination of Hydrogen Fluoride from the Electrochemical Etching of Silicon," AIChE, November 1996.

42. Scott, L.L., Bottomley, L.A., Kohl, P.A., and Winnick, J., "Electrochemical Manufacture of Sodium Dithionite," AIChE, November 1996.

43. Kohl, P. A., " Low k Dielectrics for High Speed Interconnections in Microelectronics," Invited Speaker, American Chemical Society, National Meeting, Anaheim, CA, March 22, 1999.

44. Allen, and Kohl, P. A., "Dielectric Materials, Characterization and Processing for Electronic Packaging," Second International Conference on Next Generation of Microelectronic packaging Research and Education, March 17-19, 1999.

45. Park, S., Winnick, J., and Kohl, P. A., "New Inorganic Based Electrolyte for Ambient Temperature Battery," ECS, Seattle, WA, May 1999.

46. Martin, K. P., Patel, C. S., Kohl, P. A., Ogitani, S., and Meindl, J., "Impact of Compliant Wafer Level Packaging into the Next Millennium," Semicon West, July 15, 1999.

Curriculum Vitae

L. Rafael Reif, Ph.D.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

School of Engineering Faculty Personnel Record

Full Name: L. Rafael Reif
Department: Electrical Engineering and Computer Science

Date of Birth: August 21, 1950

Citizenship: U.S.

Education:

School	Degree	Date
Universidad de Carabobo (Venezuela)	Ingeniero Electrico	Sept. 1973
Stanford University	M.S.	Oct. 1975
Stanford University	Ph.D.	Jan. 1979

Title of Thesis for Most Advanced Degree:

Doping Process in Silicon Epitaxy: Transfer Function and Physicochemical Model

Principal Fields of Interest:

Integrated circuit fabrication technology

Non-M.I.T. Experience :

Employer	Position	Beginning	Ending
MCM Electronica (Venezuela)	Engineer	Apr. 1973	June 1973
Universidad Simon Bolivar (Ven.)	Asst. Prof.	July 1973	July 1974
Stanford University	Vis. Asst. Prof.	Nov. 1978	Dec. 1979

History of M.I.T. Appointments:

Rank	Beginning	Ending
Assistant Professor	Jan. 1980	June 1983
Analog Devices Career Dev. Asst. Prof.	July 1980	June 1982
Associate Professor (without tenure)	July 1983	June 1985
Associate Professor (with tenure)	July 1985	June 1988

Professor	July 1988	–
Microsystems Technology Laboratories, Director	Sept. 1990	Jan. 1999
Department of Electrical Engineering and Computer Science, Associate Head	Jan. 1999	–

Consulting Record:

Firm	Beginning	Ending
Lincoln Laboratory	May 1980	Sept. 1983
SPIRE Corp.	Nov. 1981	Nov. 1983
Infrared Industries	Feb. 1982	
Digital Equipment Corp.	Aug. 1983	Oct. 1997
Massachusetts Technology Park Corp.	Aug. 1983	Feb. 1984
Union Carbide	Dec. 1983	
Inter-American Development Bank	Jan. 1984	Jan. 1988
Aerodyne Research	Feb. 1984	Dec. 1987
Tylan Corp.	Feb. 1984	
General Motors Research Labs	Nov. 1984	Dec. 1987
M/A Com	July 1985	
Luxembourg, Ministere des Affaires Etrangeres	Nov. 1985	Nov. 1988
Princeton Scientific Consultants	Mar. 1986	Dec. 1989
Advantage Corp.	Feb. 1987	Dec. 1990
Intel Corp.	Jan. 1988	
Matheson Gas Products	Sept. 1988	
General Electric Company	July 1989	
Applied Materials	Aug. 1994	—
Science Research Lab.	March 1994	Aug. 1995
Varian Ion Implant Systems	Sept. 1995	Dec. 1995
U.S. Venture Partners	Dec. 1995	
Morrison & Foerster	April 1996	Jan. 1997
SemiTest, Inc.	June 1996	Feb. 1999
Texas Instruments	Aug. 1996	Nov. 1996
Neo Ram	Aug. 1996	Aug. 1999
Aplex, Inc.	Jan. 1997	March 1999
Watkins Johnson	Aug. 1997	Dec. 1997
Texas Instruments	Nov. 1997	March 1999
Siemens Corp./Infineon Technologies	March 1998	December 2000
Atmel Corporation	June 1998	July 1998
Semiconductor Energy Laboratory	January 1999	—
Intel Corporation	August 1999	
UTAR Corporation	October 1999	December 2000
Micron Technology	February 2000	December 2000
SGS-Thomson Microelectronics	December 2000	February 2001
Booz Allen & Hamilton Inc.	April 2001	May 2001

Government Committees, Service, etc.:

	Beginning	Ending

National Science Foundation, Washington, DC, Ceramics and Electronic Materials/Solid State and Microstructures Small Business Initiated Research Program	Sept. 1985	
NSF Engineering Research Center for Advanced Materials Processing, North Carolina State University, Raleigh, NC, Site Visit Team	June 1993	
Massachusetts Semiconductor Industry Task Force	June 1993	June 1997
Sandia National Laboratories, Center for Microelectronics, Status Review	Feb. 1994	
National Advisory Committee on Semiconductors, Ad Hoc Working Group on University Affairs	May 1990	Dec. 1990
NSF Engineering Research Center Pre-Proposal Review Team, Washington, DC	March 1995	
National Nanofabrication Users Network, Governing Board	March 1995	March 1998
The Hong Kong University of Science and Technology, Advisory Committee, Dept. of Electrical, Electronics, and Computer Eng.	May 1995	May 2001
Semiconductor Research Corporation University Advisory Committee	Dec. 1995	Dec. 1998
Semiconductor Industry Association (SIA) Technology Strategy Committee	Jan. 1996	Jan. 1997
The Alan T. Waterman Award Committee, National Science Foundation	May 1996	May 1999
Semiconductor Research Corporation Infrastructure Task Force	Feb. 1998	May 1999
Semiconductor Research Corporation Undergraduate Scholarship Working Group	Jan. 1999	May 1999
Wearable Information Network Association	Aug. 2000	---

Editorial Board for

Journal of Electronic Materials	Jan. 1986	June 1989

Organizing Committee for:

Workshop on the Interaction of Laser Radiation with Surfaces for Application to Microelectronics, MIT, Cambridge, MA	July 1980	May 1981
1983 Electronic Materials Conference, Burlington, Vermont	Oct. 1982	June 1983
Fourth European Conference on Chemical Vapor Deposition, Eindhoven, The Netherlands	May 1983	June 1983
ECS Ninth International Conference on Chemical Vapor Deposition, Cincinnati, Ohio	May 1983	May 1984
ECS Third International Symposium on VLSI Science and Technology, Toronto, Canada	May 1983	May 1985
1984 Electronic Materials Conference, Santa Barbara, California	Oct. 1983	June 1984
ECS Fifth International Symposium on Silicon	Jan. 1984	May 1986

Materials Science and Technology, Boston, MA		
ECS Symposium on Reduced Temperature Processing for VLSI, *Co-Chairman*, Las Vegas, Nevada	May 1984	Oct. 1985
1985 Electronic Materials Conference, Boulder, Colorado	Oct. 1984	June 1985
International Electron Devices Meeting, Washington, DC	Mar. 1985	Dec. 1985
1986 Electronic Materials Conference, Amherst, MA	Oct. 1985	June 1986
ECS First International Symposium on ULSI, Philadelphia, PA	Oct. 1985	May 1987
1986 Semicon/East Technical Program, Boston, MA	Jan. 1986	Sept. 1986
1987 Semicon/East Technical Program, Chairman, Boston, MA	Sept. 1986	Sept. 1987
1987 Electronic Materials Conference, Santa Barbara, CA	Oct. 1986	June 1987
ECS Tenth International Conference on Chemical Vapor Deposition, Honolulu, Hawaii	Oct. 1986	Oct. 1987
ECS First International Symposium on Advanced Materials for ULSI, *Co-Chairman*, Atlanta, GA	Oct. 1986	May 1988
SRC Topical Research Conference on BiCMOS, *Co-Chairman*, MIT, Cambridge, MA	Sept. 1987	Dec. 1987
1988 Electronic Materials Conference	Oct. 1987	June 1988
Symposium on Novel Processing Technologies for Electronic Materials, *Chairman*, MIT, Cambridge, MA	Nov. 1987	Nov. 1988
IEEE Workshop on BiCMOS Circuits and Technology, *Co-Chairman*, New York, NY	Feb. 1988	Feb. 1989
1989 Electronics Materials Conference, MIT, Cambridge, MA	Oct. 1988	June 1989
SRC Topical Research Conference on Si-based Epitaxial Technologies, *Chairman*, MIT, Cambridge, MA	Sept. 1988	Sept. 1989
MRS Symposium on Low Temperature Si and Si-based Epitaxial Structures: Electrical Properties and Defects, *Co-Chairman*, Anaheim, CA	Feb. 1989	Feb. 1990
IEEE 1990 VLSI Technology Symposium, Honolulu, Hawaii	June 1989	June 1990
IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop, Boston, MA	Sept. 1989	Sept. 1990
IEEE 1991 VLSI Technology Symposium, Oiso, Kanagawa, Japan	June 1990	June 1991
IEEE 1992 VLSI Technology Symposium, Seattle, Washington	June 1991	June 1992
IEEE 1993 VLSI Technology Symposium, Kyoto, Japan	June 1992	June 1993
IEEE 1993 VLSI Technology Workshop, *Co-Chairman*, Kyoto, Japan	June 1992	June 1993
IEEE 1994 VLSI Technology Symposium, Honolulu, Hawaii	June 1993	June 1994
IEEE 1994 VLSI Technology Workshop, *Chairman* Honolulu, Hawaii	June 1993	June 1994

IEEE 1994 Bipolar/BiCMOS Circuits and Technology Meeting, Minneapolis, Minnesota	Oct. 1993	Oct. 1994
Miniaturization Research Committee of Foundation Advanced Technology Institute, Japan (Advisor)	Oct. 1993	Oct. 1995
TMS 1994 Electronic Materials Conference, Boulder, Colorado	Oct. 1993	June 1994
IEEE Tencon '95, Hong Kong, International Advisory Committee	Nov. 1993	Nov. 1995
IEEE 1995 VLSI Technology Symposium Kyoto, Japan	June 1994	June 1995
TMS 1995 Electronic Materials Conference, Charlottesville, Virginia (session chair)	Oct. 1994	June 1995
1996 MRS Symposium on "Environment, Safety and Health Issues in IC-production", *Co-chairman*, Boston, MA	Sept. 1995	Nov. 1996
Topical Workshop: "Economic and Technical Issues in Optimizing Plasma Processes to Minimize Environment, Safety and Health Impacts", *Co-organizer* and Session Moderator	July 1996	
IEEE 1996 VLSI Technology Symposium	June 1995	June 1996
EHS Program Committee	July 1998	———

Panelist:

Microelectronics Center of North Carolina, "Low Thermal Budget Processing"	Oct. 1985
Workshop on Foreign Participation in the SRC, Raleigh, NC	June 1990
IEEE 1990 Symposium on VLSI Technology, "Si Film and Substrate Technologies", Honolulu, Hawaii	June 1990
University of California/Los Angeles, SRC Topical Research Conference on Integration of Novel Processes	April 1991
IEEE 1993 VLSI Technology Symposium, "Surface Control for ULSI," Kyoto, Japan	May 1993
NSF Workshop on Materials for Future Electronics and Optoelectronics	Oct. 1993
Sematech President's Day, Dallas, TX	April 1996

Discussion Leader:

1984 Gordon Research Conference on "Thin Films and Solid Surfaces"	July 1984
1987 Gordon Research Conference on "Chemistry and Physics of Coatings and Films"	Aug. 1987

Awards Received:

Award	Date
Scholarship (Sears Foundation, Venezuela)	1969-1973
Outstanding Scholastic Performance (U. de Carabobo)	1973
Fellowship (Universidad Simon Bolivar)	1974-1978
IEEE Fellow	1993
1998 SRC Inventor Recognition Award	1998
2000 SRC Aristotle Award	2000

Current Organization Membership:

Organization	Offices Held
Electrochemical Society	
VLSI Processing Subcommittee of the Electronics Division	Member, May 1983 - May 1985
ULSI Processing Subcommittee of the Electronics Division	Member, May 1985 - May 1987
Symposia Planning Committee of the Electronics Division	Member, May 1983 - May 1985
Technical Planning Committee of the Electronics Division	Member, May 1985 - May 1987
Executive Committee of the Electronics Division	Consultant, May 1984 - May 1985 Member-at-large, May 1985 - May 1991 Member, May 1993 - May 1995 Member-at-Large, May 1995-May 1997 Member-at-Large, May 1997-May 1999
Metallurgical Society of AIME	
Electronic Materials Committee	Member, Mar. 1984 - June 1985 Assistant Treasurer, June 1985 - June 1987 Treasurer, June 1987 - June 1989
IEEE	Symposium on VLSI Technology, Committee Officer, June 1992-1996
American Physical Society	
Materials Research Society	
American Association for the Advancement of Science	
Tau Beta Pi	

Patents and Patent Applications Pending:

1. R. Reif, T.J. Donahue, and W.R. Burger, "Growth of Epitaxial Films by Chemical Vapor Deposition Utilizing a Surface Cleaning Step Immediately Before Deposition," U.S. Patent Number 4,579,609, April 1, 1986.

2. R. Reif and C.G. Fonstad, "Growth of Epitaxial Films by Plasma Enhanced Chemical Vapor Deposition (PE-CVD)," U.S. Patent Number 4,659,401, April 21, 1987.

3. R. Reif, P.K. Tedrow, and V. Ilderem, "Low Pressure Chemical Vapor Deposition of Refractory Metal Silicides," U.S. Patent Number 4,668,530, May 26, 1987.

4. R. Reif, C.G. Fonstad, and A.D. Huelsman, "Growth of Epitaxial Films by Chemical Vapor Deposition," U.S. Patent Number 4,773,355, September 27, 1988.

5. V. Ilderem, R. Reif, and P.K. Tedrow, "Very Low Pressure Chemical Vapor Deposition Process for Deposition of Titanium Silicide Films," U.S. Patent Number 4,957,777, September 18, 1990.

6. K.K. O, H-S. Lee, and R. Reif, "Merged Bipolar and Insulated Gate Transistors," U.S. Patent Number 5,028,977, July 2, 1991.

7. T. Noguchi, R. Reif, J.A. Tsai, and A. J. Tang, "High Performance Poly SiGe Thin Film Transistor", U.S. Patent Number 5,828,084, October 27, 1998.

8. S. Karecki, L. Pruette, and R. Reif, "Use of Non-Perfluoro Fluorocarbons for Etching and Cleaning", filed December 4, 1998 (provisional application filed December 4, 1997).

9. N. Yamauchi, J-J. J. Hajjar, and R. Reif, "Thin Film Transistor," Serial Number 07/367, 446, Filed on June 16, 1989.

Teaching Experience of L. Rafael Reif

Term	Subject Number	Title	Role
At Universidad Simon Bolivar			
SSQ73		Electronic Circuits II	Lectures, in charge
FQ73		Electronic Circuits II	Lectures, in charge
WQ74		Electronic Circuits III	Lectures, in charge
SPQ74		Electronic Circuits IV	Lectures, in charge
At MIT			
IAP80	6.151J **(NEW)**	Semiconductor Dev. Proj. Lab.	Development
ST80	6.151J	Semiconductor Dev. Proj. Lab.	Lectures
FT80	6.151J	Semiconductor Dev. Proj. Lab.	Lectures
ST81	6.151J	Semiconductor Dev. Proj. Lab.	Lectures
FT81	6.774 **(NEW)**	Integrated Circuit Fabrication Technology	Lectures, in charge development
IAP82	6.150J **(NEW)**	Introduction to Microelectronics Technology	Lectures, in charge development
ST82	6.150J	Introduction to Microelectronics Technology	Lectures, in charge
	6.151	Semiconductor Dev. Proj. Lab.	Lectures (part)
FT82	6.774	Integrated Circuit Fabrication Technology	Lectures, in charge
IAP83	6.150J	Introduction to Microelectronics Technology	Lectures, in charge
ST83	6.151	Semiconductor Dev. Proj. Lab.	Lectures (part), in charge
	6.770	Microelectronics Proj. Lab.	Lectures, in charge
	6.776J **(NEW)**	Plasma Processing in Integrated Circuit Fabrication	Lectures (part), co-in charge, development
SS83	10.61s	Plasma Processing for Micro-electronic Fabrication	Lectures, co-in charge
FT83	6.774	Physics of Microelectronic Fabrication	Lectures, in charge

ST84	6.012	Electronic Devices and Circuits	Recitation (2 sections)
SS84	10.61s	Plasma Processing for Micro-electronic Fabrication	Lectures, co-in charge
FT84	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
ST85	6.776J	Plasma Processing in Integrated Circuit Fabrication	Lectures, co-in charge
SS85	10.61s	Plasma Processing for Microelectronic Fabrication	Lectures, co-in charge
FT85	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
ST86	6.002	Circuits and Electronics	Recitation (2 sections)
SS86	10.61s	Plasma Processing for Microelectronic Fabrication	Lectures, co-in charge
FT86	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
ST87	6.776J	Plasma Processing in Integrated Circuit Fabrication	Lectures, co-in charge
SS87	10.61s	Plasma Processing for Microelectronic Fabrication	Lectures, co-in charge
FT87	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
SS88	10.61s	Plasma Processing for Microelectronic Fabrication	Lectures, co-in charge
FT88	6.774	Physics of Microelectronic Fabrication	Lectures, co-in charge
ST89	6.776J	Plasma Processing in Integrated Circuit Fabrication	Lectures, co-in charge
SS89	10.61s	Plasma Processing for Microelectronic Fabrication	Lectures, co-in charge
FT89	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
SS90	10.61s	Plasma Processing for Microelectronic Fabrication	Lectures, co-in charge

FT90	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
ST91	6.776J	Plasma Processing in Integrated Circuit Fabrication	Lectures, co-in charge
SS91	10.61s	Plasma Processing for Microelectronic Fabrication	Lectures, co-in charge

FT91	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
SS92	10.61s	Plasma Processing for Microelectronic Fabrication	Lectures, co-in charge
FT92	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
ST93	6.776J	Plasma Processing in Integrated Circuit Technology	Lectures, co-in charge
SS93	10.61s	Plasma Processing for Microelectronic Fabrication	Lectures, co-in charge
FT93	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
SS94	10.61s	Plasma Processing for Microelectronic Fabrication	Lectures, co-in charge
FT94	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
ST95	6.776J	Plasma Processing in Integrated Circuit Technology	Lectures, co-in charge
SS95	10.61s	Plasma Processing for Microelectronic Fabrication	Lectures, co-in charge
FT95	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
ST96	6.012	Electronic Devices and Circuits	Recitation (1 section)
SS96	6.74s **(NEW)**	Multilevel Interconnect Process Technologies for Microelectronics Fabrication	Lectures, in charge, development
FT96	6.973 **(NEW)**	Physics of Microelectronic Fabrication: Back End Processing	Lectures, in charge, development
SS97	6.74s	Multilevel Interconnect Process Technologies for Microelectronics Fabrication	Lectures, in charge,
FT97	6.774	Physics of Microelectronic Fabrication	Lectures, in charge
SS98	6.74s	Multilevel Interconnect Process Technologies for Microelectronics Fabrication	Lectures, in charge,

SS99	6.74s	Multilevel Interconnect Process Technologies for Microelectronics Fabrication	Lectures, in charge,
SS00	6.74s	Multilevel Interconnect Process Technologies for Microelectronics Fabrication	Lectures, in charge,

Other Teaching Experience

"Applied Materials Technology," offered at Materials Processing Center, MIT, Cambridge, MA by IBM. In charge of four 1.5-hour sessions, June 20 - July 1, 1983.

"Physics of Microfabrication," offered by Digital Equipment Corporation, Hudson, MA. In charge of five all-day sessions, from 8:30-4:00, August 22-26, 1983.

"Applied Materials Technology," Course 3.07s by Summer Session Program, MIT, Cambridge, MA. In charge of two 1.5-hour sessions, June 11-22, 1984.

"Physics of Microelectronic Fabrication," offered by Digital Equipment Corporation, Hudson, MA. In charge of five all-day sessions, from 8:30-4:00, July 30-August 3, 1984.

"Plasma Processing for Microelectronic Fabrication," offered by Digital Equipment Corporation, Hudson, MA. Co-in charge of five all-day sessions, from 8:30-4:00, March 25-29, 1985.

"Applied Materials Technology," Course 3.07s by Summer Session Program, MIT, Cambridge, MA. In charge of two 1.5-hour sessions, June 10-21, 1985.

"Physics of Microfabrication," offered by Digital Equipment Corporation, Hudson, MA. In charge of five all-day sessions, from 8:30-4:00, August 26- 30, 1985.

"Plasma Processing for Microelectronic Fabrication," offered by Digital Equipment Corporation, Hudson, MA.. Co-in charge of five all-day sessions, from 8:30-4:00, March 24-28, 1986.

"Plasma Enhanced Chemical Vapor Deposition of Thin Films for Microelectronics," offered by Materials Research Society. In charge of one all-day session, from 8:30-4:00, April 18, 1986, Palo Alto, CA.

"Plasma Processing," offered by IBM Corp., Thornwood, NY. In charge of one 1.5-hour session, July 21, 1986.

"Physics of Microfabrication," offered by Digital Equipment Corporation, Hudson, MA. In charge of five all-day sessions, 8:30-4:00, August 25-29, 1986.

"CVD and Plasma Enhanced CVD," offered by Princeton Scientific Consultants, Inc.
In charge of one half-day session, 9:00-12:00, October 2, 1986, Princeton, NJ.

"Plasma Enhanced Chemical Vapor Deposition of Thin Films for Microelectronics," offered by Materials Research Society. In charge of one all-day session, 8:30-4:00, December 5, 1986, Boston, MA.

"Silicon Epitaxy for VLSI," offered by U.C. Berkeley. In charge of two 1.5- hour sessions, February 3, 1987, Palo Alto, CA.

"Plasma Enhanced Chemical Vapor Deposition of Thin Films for Microelectronics," offered by Materials Research Society. In charge of one all-day session, 8:30 - 4:00, April 24, 1987, Anaheim, CA.

"CVD and Plasma Enhanced CVD," offered by Princeton Scientific Consultants, Inc. In charge of one half-day session, 1:00 - 5:00, June 8, 1987, Lambertville, NJ.

"Physics of Microfabrication," offered by Digital Equipment Corporation, Hudson, MA. In charge of five all-day sessions, August 24-28, 1987.

"Plasma Enhanced Chemical Vapor Deposition of Thin Films for Microelectronics," offered by Materials Research Society. In charge of one all-day session, 8:30-4:00, November 30, 1987, Boston, MA.

"Plasma Processing for Microelectronic Fabrication," offered by Intel Corp., Santa Clara, CA. Co-in charge of five all-day sessions, 8:30-4:00, January 1988.

"Silicon Epitaxy for VLSI," offered by U.C. Berkeley. In charge of three 1.5-hour sessions, August 4-5, 1988, Palo Alto, CA.

"CVD and Plasma Enhanced CVD," offered by Princeton Scientific Consultants, Inc. In charge of one half-day session, 1:00-5:00, November 14-16, 1988.

"Plasma Processing for Microelectronic Fabrication," offered by Digital Equipment Corporation, Hudson, MA. Co-in charge of five all-day sessions, 8:30-4:00, November 22-December 21, 1988.

"Plasma Enhanced Chemical Vapor Deposition of Thin Films for Microelectronics," offered by Materials Research Society. In charge of one all-day session, 8:30-4:00, December 2, 1988, Boston, MA.

"CVD and Plasma Enhanced CVD," offered by Princeton Scientific Consultants, Inc. In charge of one half-day session, 9:00-12:00, March 13-15, 1989, Princeton, NJ.

"Physics of Microfabrication," offered by Digital Equipment Corporation, Hudson, MA. In charge of five all-day sessions, 8:30-4:00, June 12-28, 1989.

"Plasma Processing for Microelectronic Fabrication," offered by Digital Equipment Corporation, Hudson, MA. Co-in charge of five all-day sessions, 8:30-4:00, November 16-22, 1989.

"Physics of Microfabrication," offered by Digital Equipment Corporation, Hudson, MA. In charge of twenty two-hour sessions, February 8-May 3, 1990.

"Plasma Processing for Microelectronic Fabrication," offered by Digital Equipment Corporation, Hudson, MA. Co-in charge of five all-day sessions, 8:30-4:00, February 13-22, 1991.

"Physics of Microfabrication," offered by Digital Equipment Corporation, Hudson, MA. In charge of five all-day sessions, 8:30-4:00, October 30 - November 8, 1991.

"Plasma Processing for Microelectronic Fabrication," offered by Intel Corp., Santa Clara, CA. Co-in charge of five all-day sessions, 8:30-4:00, July 1992.

"Physics of Microfabrication," offered by Digital Equipment Corporation, Hudson, MA. In charge of five all-day sessions, 8:30-4:00, November 29 - December 17, 1993.

"Defect Reduction and Yield" offered by Digital Equipment Corporation, Hudson, MA. In charge of five all-day sessions, 8:30-4:00, June 5-16, 1995.

"Defect Reduction and Yield" offered by Digital Equipment Corporation, Hudson, MA. In charge of five all-day sessions, 8:30-4:00, December 14-22, 1995.

"Defect Reduction and Yield" offered by Digital Equipment Corporation, Hudson, MA. In charge of five all-day sessions, 8:30-4:00, May 27-June 7, 1996.

"Multilevel Interconnect Process Technologies for Microelectronic Fabrication", offered by Intel Corporation, Rio Rancho, NM. In charge of five all-day sessions, 9:00-4:00, August 16-20, 1999.

"Plasma Etching for Silicon Microfabrication", offered by Chartered Semiconductor Mfg Ltd., Singapore. In charge of two all-day sessions, 9:00-4:00, July 17-18, 2000.

Publications of L. Rafael Reif

1. Books/Chapters

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* 42. Karecki, S.M., L.C. Pruette, R. Reif, T. Sparks, L. Beu, and V. Vartanian, "Use of Alternative Chemistries for a Silicon Dioxide Etch Application in an Applied Materials Centura 5300 HDP Etch Tool" (***invited paper***), Proceedings of the SEMI Technical Program: A Partnership for PFC Emissions Reductions, SEMICON/Southwest 1997, Austin, TX, October 13, 1997, p. F-1.

* 43. Karecki, S.M., L.C. Pruette, R. Reif, "..." (***invited paper***), 1998 Schumacher Symposium, March 2-4, 1998, San Diego, CA.

* 44. Karecki, S., R. Chatterjee, L. Pruette, R. Reif, T. Sparks, L. Beu, and V.Vartanian, "Reduction of Global Warming Emissions in a Dielectric Etch Application through Use of Iodofluorocarbon Chemistry," Proceedings of the SEMI Technical Program: A Partnership for PFC Emissions Reductions, SEMICON/Southwest 1998, Austin, TX, October 19, 1998, p. I-1.

* 45. Karecki, S., L. Pruette, R. Chatterjee, and R. Reif, "Alternative Chemistries

for Dielectric Etch Processes" (***invited talk***), Northern California Chapter of the American Vacuum Society Plasma Etch Users Group Meeting, Santa Clara, CA, March 2, 1999.

*46. R. Chatterjee, S. Karecki, R. Reif, T. Sparks, V. Vartanian, and Brian Goolsby, "The Use of C_4F_6 for Dielectric Etch with Reduced Global Warming Emissions," Proceedings of the SEMI Technical Program: A Partnership for PFC Emissions Reductions, SEMICON/Southwest 2000, Austin, TX, October 16, 2000.

*47. Reif, R., "Future Technologies to Interface with Nature," **(invited article)** Nature Interface (Japan), pp. 16-18, Vol. 1, No. 1, January 2001.

*48. R. Chatterjee, R. Reif, T. Sparks, Brian Goolsby, V. Vartanian, and L. Mendicino, "Tetrafluoroethylene Based Dielectric Etch Processes for Reduced Global Warming Emissions on a High Density Plasma Chamber," Proceedings of the SEMI Technical Program: A Partnership for PFC Emissions Reductions, SEMICON/Southwest 2001, Austin, TX, October 15, 2001.

5. **Internal Memoranda and Progress Reports**

6. **Invited Lectures**

July 1979, "Chemical Vapor Deposition of Epitaxial Silicon," Workshop on Computer Aids for IC Technology and Device Design, Stanford University, Stanford, CA.

September 1981, "Silicon Epitaxy and Thin Gate Dielectrics for VLSI," CNET, Centre de micro-electronique de Grenoble, Grenoble, France.

May 1982, "Thin Silicon Films for Microelectronic Applications," Industrial Liaison Symposium on Electronic Materials and Devices, MIT, Cambridge, MA.

May 1982, "Thin Silicon Films for Microelectronics," IBM, T.J. Watson Research Center, Yorktown Heights, NY.

July 1982, "Plasma Assisted CVD of Thin Silicon Films," US-German Workshop on Fundamental Problems in VLSI Processing, Munich, Germany.

July 1982, "Low Temperature Silicon-on-Insulator Technology," US-German Workshop on Fundamental Problems in VLSI Processing, Munich, Germany.

February 1983, "Thin Silicon Films for Microelectronic Applications," Digital Equipment Corporation, Hudson, MA.

April 1983, "Plasma Assisted Chemical Vapor Deposition of Thin Films for VLSI Applications," IEEE Meeting on Computers and Technology, Poughkeepsie, NY.

May 1983, "Low Temperature Epitaxial Deposition of Solid Silicon by Plasma Enhanced CVD," US Army Armament Research and Development Command, Dover, NJ.

June 1983, "Properties of Thin Polycrystalline Silicon Films Deposited by Plasma-Assisted CVD," Rheinisch-Westfalischen Tech. Hochschule, Aachen, W. Germany.

September 1983, "Requirements for Low Temperature Processing," Semicon/East Technical Program, Boston, MA.

November 1983, "Plasma Enhanced CVD of Silicon Epitaxy and Refractory Metal Silicides," Semiconductor Research Corporation, Deposition Processes Topical Research Conference, RPI Center for Integrated Electronics, Watervliet, NY.

December 1983, "Plasma Enhanced Chemical Vapor Deposition in Microelectronics," Union Carbide, Tarrytown, NY.

February 1984, "Low Temperature VLSI Processing and Process Modeling," Industrial Liaison Symposium on Electronic Materials Processing, MIT, Cambridge, MA.

March 1984, "Plasma Enhanced CVD of Thin Films," Symposium n Dry-Processing Science and Technologies, RCA Laboratories, Princeton, NJ.

September 1984, "Low Temperature Processing," ASM Materials Science Seminar on Advances in Electronic Materials, Detroit, MI.

November 1984, "Plasma Enhanced Chemical Vapor Deposition," New England Chapter of the American Vacuum Society, Burlington, VT.

November 1984, "Low Temperature Processing for VLSI," General Motors Research Laboratories, Warren, MI.

January 1985, "CVD of Si Epitaxy for VLSI," 1985 Advanced Semiconductor Equipment Exposition's Technical Conference on Manufacturing Science, San Jose, CA.

February 1985, "Low Temperature Silicon Epitaxy for VLSI," Texas Instruments Inc., Dallas, TX.

March 1985, "Very Low Pressure Chemical Vapor Deposition of Silicon Epitaxy and Titanium Silicide Films," GTE Laboratories Inc., Waltham, MA.

June 1985, "Plasma Enhanced Chemical Vapor Deposition of Silicon Epitaxial Films," 1985 IBM Plasma Symposium, Burlington, VT.

June 1985, "Plasma Enhanced Chemical Vapor Deposition of Low-Temperature Silicon Epitaxial Films," Annual Symposium of the New England Combined Chapter of the American Vacuum Society, Nashua, NH.

June 1985, "Very Low Pressure Chemical Vapor Deposition of Silicon Epitaxial Films," Whitney Symposium on Science and Technology VI, General Electric, Schenectady, NY.

December 1985, "Low Temperature Processing for Microelectronics," Symposium Diamonds in the Sand, Dedication of the G.S. Brown Building, MIT, Cambridge, MA.

January 1986, "Low Temperature Microelectronics Processing," MIT Industrial Liaison Symposium on Recent Advances in VLSI, Santa Clara, CA.

February, 1986, "Low Temperature Epitaxial Silicon Deposited by Plasma-Enhanced Chemical Vapor Deposition," Engineering Foundation Conference on Processing of Electronic Materials, Santa Barbara, CA.

March, 1986, "Low Temperature Silicon Epitaxy by Plasma Enhanced Chemical Vapor Deposition," IBM T.J. Watson Research Center, Yorktown Heights, NY.

April 1986, "Low Temperature Silicon Epitaxial Growth by Plasma Enhanced ChemicalVapor Deposition," AT&T Bell Laboratories, Murray Hill, NJ.

May 1986, "Novel Processing Technologies for VLSI," Eastman Kodak Research Laboratories, Rochester, NY

May 1987, "Recent Developments in Thin Film Technology Research," General Motors Research Laboratories, Warren, MI.

May 1987, "Processing of Thin Films for Microelectronics," Industrial Liaison Symposium on Surfaces and Interfaces, MIT, Cambridge, MA.

June 1987, "Recent Developments in Low Temperature Silicon Epitaxy by Plasma-CVD," Annual Symposium of the New England Combined Chapter of the American Vacuum Society, Newton, MA.

September 1987, "Plasma Enhanced Deposition of Epitaxial Si and GaAs," GTE Research Laboratories, Waltham, MA.

September 1987, "Plasma Enhanced Deposition of Epitaxial Si and GaAs," Raytheon Research Division, Lexington, MA .

July 1988, "Recent Developments in Low Temperature Si Epitaxy for High Speed Bipolar Applications," IBM East Fishkill, NY.

November 1988, "Recent Developments in Low Temperature Si Epitaxy," Delco Electronics, Kokomo, IN.

December 1988, "Recent Advances in Low Temperature Si Epitaxy by CVD," Texas Instruments, Dallas, TX.

April 1989, "Novel Device Fabrication and Processing," Industrial Liaison Symposium on Recent Advances in VLSI, MIT, Cambridge, MA.

May 1990, "Recent Developments in Low Temperature Si Epitaxy by CVD," North Carolina State University, NC.

August 1990, "Recent Developments in Low Temperature Si Epitaxy by CVD," NTT Musashino, NTT Atsugi, and Hitachi CRL, Japan.

June 1991, "Recent Advances in the CVD of Epitaxial Si: In-Situ Monitoring and Si-Ge," Fujitsu, NTT Atsugi, Toshiba, NEC, and Kanazawa University, Japan.

November, 1991, "New Developments in the CVD of Semiconductor Thin Films: Si-Ge and Real Time, In-Situ Monitoring," Columbia University, NY.

April, 1992, "New Developments in the Chemical Vapor Deposition of Semiconductor Thin Films: $Si_{1-x}Ge_x$ and In-Situ Real Time Monitoring," AT&T Bell Laboratories, Murray Hill, NJ.

May, 1992, "New Developments in the Chemical Vapor Deposition of Semiconductor Thin Films: $Si_{1-x}Ge_x$ and In-Situ , Real-Time Monitoring," Industrial Liaison Symposium on Electronic Materials: Synthesis and Control of Structure from Atoms to Devices, MIT, Cambridge, MA.

November, 1992, "In-Situ, Real-Time Monitoring of CVD Si Epitaxy," Sematech, Austin, TX.

Decemb r, 1992, "Si-Ge Heteroepitaxy by Very-Low-Pressure Chemical Vapor Deposition," Nippon-Sanso Ninth Annual Process Seminar, Semicon Japan, Chiba, Japan

March, 1993, "Overview of Microsystems Technology Laboratories," Motorola, Austin, TX.

March, 1993, "In-Situ, Real-Time Monitoring of Epitaxial Film Growth in a CVD Reactor," Texas Instruments, Dallas, TX.

January, 1994, "New Developments in the Chemical Vapor Deposition of Semiconductor Thin Films: Si-Ge and *In-situ*, Real-time Monitoring," Digital Equipment Corp., Hudson, MA.

September, 1994, "Overview of Microsystems Technology Laboratories", Motorola, Phoenix, AZ.

September, 1994: "Polycrystalline Silicon-Germanium for Thin Film Transistors", Motorola, Phoenix, AZ.

March, 1995: "Alternative Chemistries for Wafer Etching and PECVD Chamber Cleaning," Digital Equipment Corporation, Hudson, MA.

February, 1996: "Recent Advances at MIT's Microsystems Technology Laboratories," Rockwell, Newport Beach, CA.

March, 1996: "University Networks of Excellence: A New Component of the Research Infrastructure," Semiconductor Technology Council, Washington, DC.

April, 1996: "Advances in Microsystems Technology," Forum Comissionat per a Universitats I Recerca, Barcelona, Spain.

September, 1996: "Plasma Issues in new ERC on Environment, Safety and Health in Semiconductor Manufacturing," Tucson, AZ.

September, 1996: "Recent Advances at MIT's Microsystems Technology Laboratories", Lucent Technologies, Murray Hill, NJ.

January, 1997: "Made By Hong Kong: Electronics Sector," Hong Kong

January, 1997: "Environmental, Safety, and Health Issues in IC Manufacturing," ESH/ERC Videoconference Series, MIT, Cambridge, MA.

July, 1997: "Environmentally Benign Semiconductor Manufacturing," National University of Singapore, Singapore.

March, 1999: "Environmentally Benign Semiconductor Manufacturing," EECS Colloquium, MIT, Cambridge, MA.

June, 2000, "Plasma Etching Processes for the Reduction of Global Warming Emissions, and Monolithic Three Dimensional Integration in Microelectronics," Technion-Israel Institute of Technology, Haifa, Israel.

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EXHIBIT C